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LEAKAGE CURRENT CONTROLLING MECHANISM USING HIGH K DIELECTRIC + METAL GATE

Abhishek Kumar

ABSTRACT: In this paper we analyze the use of Metal gate and High K dielectric for future transistor. Leakage current is the main cause of transistor with Sio2 dielectric, In order to control the leakage current high-K dielectric with metal gate has been reported. For the continued scaling Sio2 dielectric is replace with high-k dielectric and found that 300 times improvement in leakage current as well as 100 times improvement in ON/OFF ration. The most promising candidate (AI2O3) has been found. AI2O3 also show the steeper Subthreshold swing curve (Faster ON-OFF switching) compare to Sio2.

Keywords: MOSFET, High–K Dielectric, Metal gate, Sub threshold Swing, leakage current.

1. INTRODUCTION

MOSFET is the one of the most preferred transistor due to its unique property of scaling. Scaling allows reducing the device size by all around without affecting the performance. Silicon is the most preferred semiconductor due to silicon oxide. Silicon dioxide is the key reason that micro-electronics technology uses Si and not some other semiconductor. Si is an average semiconductor in performance, but in all other aspects SiO2 is an excellent insulator. SiO2 has the key advantage that it can be made from Si by thermal oxidation, whereas every other semiconductor has a poor native oxide. SiO2 is amorphous has very few electronic defects and forms an excellent interface with Si. Scaling is the unique property of MOSET it allow to reduce the size nano scale region. Scaling enables the reduction in dimension in all aspect but scaling cannot go on forever. There is limit of scaling beyond that the device does incorporate unexpected result. The SiO2 gate oxide has been serving as the key enabling material in scaling silicon CMOS technology. However continued gate oxide scaling is becoming exceedingly difficult since (a) the gate oxide leakage is increasing with decreasing SiO2 thickness and (b) SiO2 is running out of atoms for further scaling.

Scaling of gate length and gate oxide is most interested scalable dimension since last decade. This improves the control of the gate electrode over the channel enabling both shorter channel lengths and higher performance. As the gate oxide was scaled the gate leakage increased; this increase in gate leakage was insignificant until the 90nm technology node. At the 90nm and 65nm nodes the scaling of the gate oxide slowed as a result of the power limitations from the increase in gate leakage. In order to overcome this at the 45nm technology, a gate dielectric with a higher dielectric constant (high-k) has been introduced. This enabled a >25x gate leakage reduction while scaling the gate oxide thickness (Tox) by 0.7x.

The introduction of high-k gate dielectrics has been showed the transistor by several issues. The interaction by the high-k material with the existing polysilicon gates. This interaction led to high trap densities at the interface that reduced the Vth of the transistor. The second was the degradation of the channel mobility in the presence of high-k dielectrics. The third issue was the poor reliability of the high-k dielectric. High-k + metal gate a key requirement of the technology node. Replacement of SiO2, the workhorse of the industry for over 30 years, with a high-K dielectric will be required. Other changes will include use of raised source/drain, metal gate electrodes and channel engineering.

2. NEED OF HIGH-K DIELECTRIC

The dielectric constant k is a parameter defining ability of material to store charge. Consequently it also defines capacitance C of any capacitor comprising of a layer of dielectric sandwiched between two metal plates. In the figure 1 below size of the upper plate defines area of the capacitor contact (A).

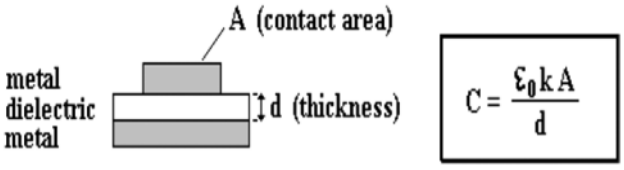

Figure 1: Capacitance of a Dielectric.

Where ε0 is the permittivity of free space, K is the relative permittivity, A is the area and t is the SiO_2 thickness. K would determine capacitance of the above structure or in other words it would define the extent of capacitive coupling between two conducting plates – with "high"-k dielectric

[1] Electronics and Communication Department, Lovely Professional University, Phagwara, Jalandhar, India, E-mail: abhishek.15393@lpu.co.in.

such coupling would be strong and with "low"-k dielectric being obviously weak. In Si technology the reference is a value of k of silicon dioxide, SiO2, which is 3.9. Dielectrics featuring k>3.9 are referred to as "high"-k dielectric while dielectric featuring k<3.9 are defined as "low"-k dielectrics.

The requirements of a new oxide are six-fold:

1. It must have a high enough K.
2. The oxide is in direct contact with the Si channel.
3. It must be kinetically stable.
4. It must act as an insulator.
5. It must form a good electrical interface with Si.
6. It must have few bulk electrically active defects.

In MOS transistor Current flows from source to drain when gate is at certain voltage otherwise it doesn't flow. NMOS transistors are on when gate is at high when voltage; PMOS transistors are on when gate is at when low voltage. Silicon dioxide has been used as a gate oxide material for decades. As transistors have decreased in size the thickness of the silicon dioxide gate dielectric has steadily decreased to increase the gate capacitance and drive current and device performance. As the thickness scales below 2 nm leakage currents due to tunnelling increase drastically, leading to unwieldy power consumption and reduces device reliability. Decreasing channel length lowers the threshold voltage Vth.

To reduce the leakage current researchers have shown that by replacing the SiO2 dielectric by a higher K dielectric value has much better result. Its (SiO2) only problem is that when very thin it is possible to tunnel across it. Hence we must loose these advantages of SiO2 and start to use a new high K oxide. Replacing the silicon dioxide gate dielectric with a high-k material allows increased gate capacitance without the concomitant leakage effects. Physically two changes have been made; in conventional transistor (1) a polysilicon gate is used to interconnect with gate material, while a high K transistor metal gate is used to interconnect the high k dielectric. (2) SiO2 dielectric has been replaced with High K dielectric layer. This transistor have been called High K-Metal gate transistor and it is most preferred for nano scale transistor.

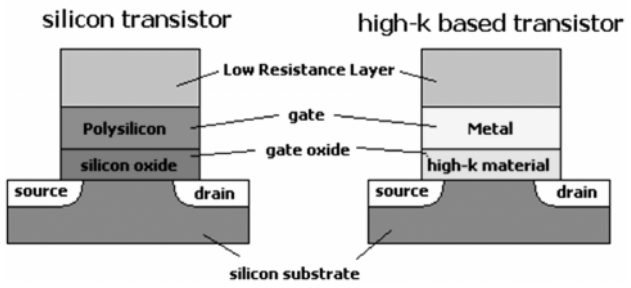

Figure 2: Position of High-K and Metal Gate.

According to Moore's law of scaling "the device performance in the 21st century high-κ gate dielectrics and metal gate electrodes will be required for high-performance and low-power CMOS applications in the 45 nm node and beyond". Metal gates with "correct" work functions can be used to provide the right transistor threshold voltages, alleviate the mobility degradation problem and enable high-performance high-κ/metal gate transistors with low gate dielectric leakages for future logic applications. High-κ gate dielectrics and metal gates are required for the successful demonstration of high performance logic transistors on high-mobility non-silicon gate material with high ION/IOFF ratios.

With respect to other sources of leakage, gate-oxide scaling has long been considered an eventual limiter for gate oxides below ~2nm gate dielectric thickness. It is felt that with oxides reaching the thickness of several atoms gate leakage would rival and would surpass the transistor off-current leakage. Research on high-K dielectrics for MOS transistor applications has become an area of active research. The reason for this is shown in Figure 3 [5]. It can be seen here that for the same equivalent oxide thickness (the thickness that SiO2 would have for a given capacitance value) the high-k dielectric has more than four orders of magnitude less gate leakage than SiO2.

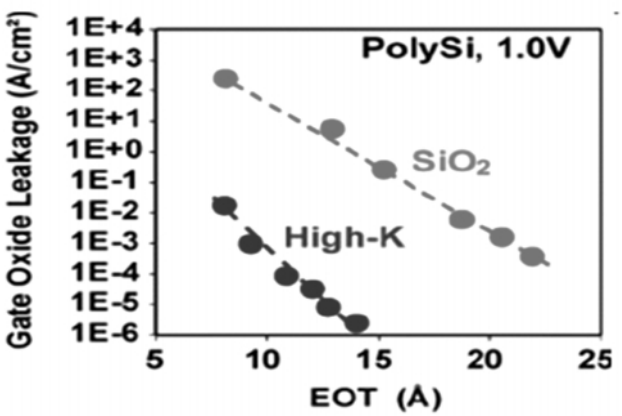

Figure 3: Comparison of Gate Leakage Between SiO2 and High-K Dielectrics [5].

Si3N4 and Al2O3-based high-κ gate dielectric materials are discussed in this paper. The choice between poly-Si or a metal as the gate electrode for the high-κ dielectric is crucial. The combination of a high-κ dielectric and a poly-Si gate is not suitable for high performance logic applications since the resulting high-K/poly-Si transistors have high threshold voltages and degraded channel mobility. Metal gates with "correct" work functions can be used to provide the right transistor threshold voltages. For conventional planar CMOS applications on bulk silicon, a p+ metal work function is needed for the PMOS transistor while an n+ metal work function is required for the NMOS transistor in order to satisfy the correct transistor threshold voltages.

Table 1
List of High-k Dielectric

High-K Material	K-value	Gap (eV)
Si	3.9	1.1
SiO2	3.9	9
Si3N4	7	5.3
Al2O3	9	8.8
Ta2O5	22	4.4
TiO2	80	3.5
ZrO2	25	5.8
HfO2	25	5.8

High-k dielectrics are needed in MOS gate stacks to maintain sufficiently high capacitance of the metal (gate)-dielectric-Si structure in MOS/CMOS transistors. The term high-K dielectric refers to a material with a high dielectric constant K (as compared to silicon dioxide) used in semiconductor manufacturing processes which replaces the silicon dioxide gate dielectric. Replacing the silicon dioxide gate dielectric with a high-K material allows increased gate capacitance without the concomitant leakage effects. The high-K-metal gate combination is important for enabling future high-performance and low gate leakage emerging nano transistors. The high-k + metal gate transistors exhibit excellent NMOS and PMOS short channel effects (SCE) and drain induced barrier-lowering (DIBL) due to the combination of Tox scaling and the optimal work function metal gates.

3. RESULT AND DISCUSSION

In this section, we analyze the effect of high K dielectric on the Voltage-current characterices and leakage current of transistor. High K dielectric shows the significance improvement in leakage current. Fig. 4 VI-characterices of transistor at different K value at their appropriate work function. As the k value increases the curve tends to fall downward and current decreases drastically. Fig. 4 shows the VI curve of NMOS, current should flow when Vg > Vth (Vth is a positive number) but there is a small current gate voltage less than threshold voltage. In saturation region negligible current flow. At Vg = 0v; for K = 3.9 Id 1e – 5 to K = 10 Id = 1e–20. From the fig. 4 it is observe that for the same gate voltage the improvement in off current 300% when the K value increases from 3.9 to 10. Blue color shows line at Vd = 0.05v and red color shows at Vd = 1.0v. The curve have been drawn for 4 different dielectric value, k = 3.9 (SiO2) k = 7 (Si3N4) k = 9 (Al2O3) and k = 10.

The fig. 5 shows the off state current curve at different k value. For the SiO2 (K = 3.9) the curve follow the straight line equation with constant slope. As the k value increases the off current falls horizontally and almost zero. With SiO2 layer the off current at drain voltage 0 volts is 0.75 μA, for the higher K value (K = 7, 9, 10) the off current is around 7.5 nA (almost negligible). In Sio2 layer the off current increases linearly with drain voltage while for high K dielectric off current is constant and it is independent of drain voltage. A high K dielectric shows 100 time improvement in off current.

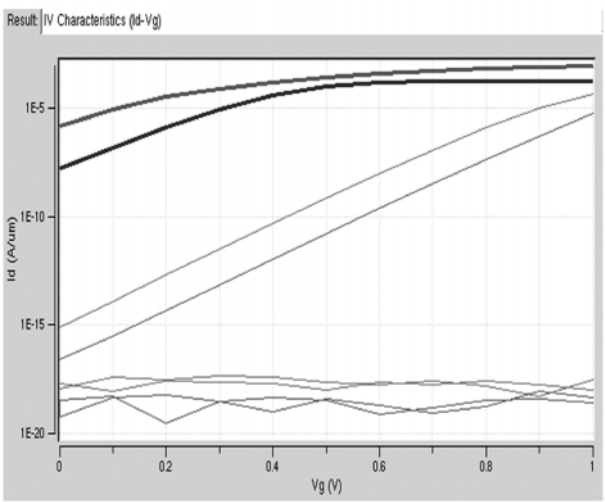

Figure 4: VI Characterics for K = 3.9, 7 and 9.

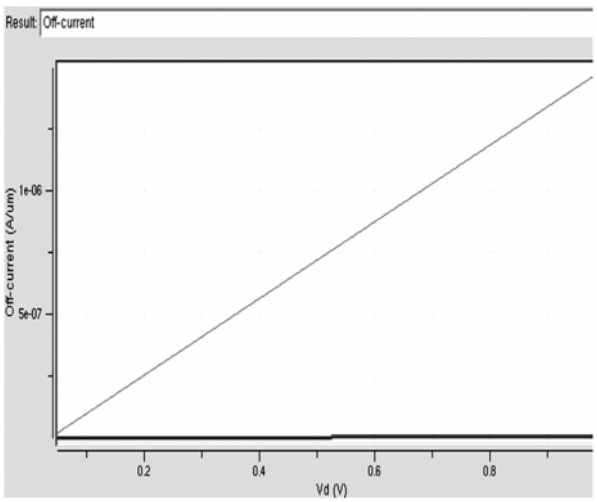

Figure 5: Leakage Current Curve for K = 3.9, 7 and 9.

4. SUB THRESHOLD SWING

Sub threshold swing is an important device characteristic in sub threshold region. The Parameter to quantify how sharply the transistor turned off by gate voltage is called sub threshold swing. Sub threshold swing is defined as the gate voltage Vgs needed in order to induce drain current Ids change of one order of magnitude. In the sub threshold region the drain current behavior is similar to the exponentially increasing current of a forward biased diode. The plot of logarithmic drain current versus gate voltage with drain, source and bulk voltages fixed will exhibit approximately linear behavior in the MOSFET operating

regime. Its slope is the subthreshold slope. A device characterized by steeper subthreshold slope exhibits a faster transition between off (low current) and on (high current) state. Smaller the value of S better turn ON performance of the device. The subthreshold slope reciprocal value called subthreshold swing S which is usually given as

$$Ss - th = \ln(10)\frac{kt}{q} + \left(1 + \frac{Cd}{Cox}\right)$$

C_d = depletion layer capacitance.

C_{ox} = gate-oxide capacitance.

The typical value of Sub threshold swing at room temperature is 70mV/dec. Fig. 6 shows the subthreshold Swing for different k value. For K 3.9 and 9 the curve is steeper while for k = 7 the curve is almost horizontal. A steeper sub threshold swing curve gives minimum leakage current, so we can analyze that leakage current is minimum for Al2O3 (k = 9) and it best suited dielectric for nano transisitor.

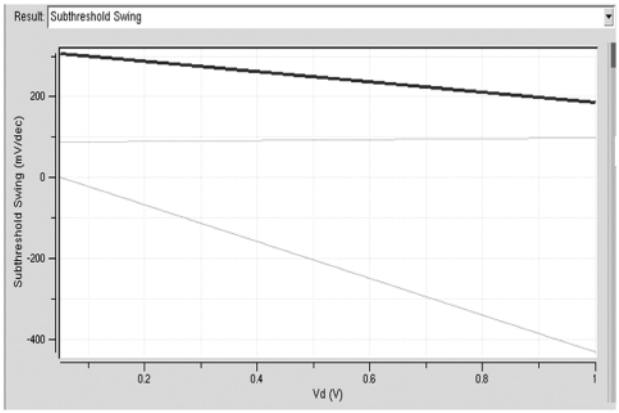

Figure 6: Subthreshold Swing for K = 3.9, 7 and 9.

5. CONCLUSION

For both future silicon and emerging non-silicon nanoelectronic transistors leakage current and off state current is most limiting factor. To achieve higher performance changes have been made architecture level, replacement of Sio2 dielectric with high-K dielectric and use of metal gate instead of poly gate. The use of a high-κ gate dielectric between the metal gate and the III-V device layers will eliminate such leakage and potentially improve the ION /IOFF ratio. The simulation result shows the Improvement in leakage current is 300 times and off state current 100 times. Subthreshold which determine the speed of ON-OFF state switching, has been illustrated for different K-value, AL_2O_3 has been found that faster switching speed. For future scaling the transistor architecture must includes high-K dielectrics if gate capacitance scaling is to continue down to 10nm gate lengths.

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