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Analysis of Cascaded Integrator Comb (CIC) Decimation Filter in Efficient Compensation

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Abstract: Decimation filter has wide application in both the analog and digital system for data rate conversion as well as filtering. In this paper, we have discussed about efficient structure of a decimation filter. We have three class of filters FIR, IIR and CIC filters. IIR filters are simpler in structure but do not satisfy linear phase requirements which are required in time sensitive features like a video or a speech. FIR filters have a well defined frequency response but they require lot of hardware to store the filter coefficients. CIC filters don't have this drawback they are coefficient less so hardware requirement is much reduced but as they don't have well defined frequency response. So another structure is proposed which takes advantage of good feature of both the structures and thus have a cascade of CIC and FIR filters. They exhibit both the advantage of FIR and CIC filters and hence more efficient over all in terms of hardware and frequency response requirements.

Keywords: Multirate Filtering, Decimation, Sampling rate conversion, Compensation Theory

1. INTRODUCTION

Fast sampling rates offer several benefits, including the ability to digitize wideband signals, reduced complexity of anti-alias filters, and lower noise power spectral density. The result is improved SNR in the system. Digital filtering is a computational process used for transforming a discrete sequence of numbers (the input) into another discrete sequence of numbers (the output) having a modified frequency domain spectrum. Digital filtering algorithms are most commonly implemented using general purpose digital signal processing chips for higher sampling rates.

The decimation filter (decimator) is one of the basic building blocks of a sampling rate conversion system. The decimation filter performs two operations: low-pass filtering as well as down-sampling. The filter converts low resolution high bit-rate data to high resolution low frequency data. It has been widely used in such applications as speech processing, radar systems, antenna systems and communication systems. Considerable attention has been focused in the last few years on the design of high efficiency decimation filters.

In 1981, Eugene Hogenauer [1] invented a new class of economical digital filters for decimation and interpolation (converting the sampling rate from low to high) called a cascaded integrator comb (CIC) filter. This filter was composed of an integrator part and a comb part. No multipliers were required and the storage requirement was reduced when compared with other implementations of decimation filters. The CIC filter can also be implemented very efficiently in hardware due to its symmetric structure.

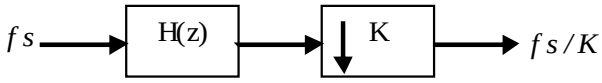


Figure 1: Conceptual View of a Decimation Filter

This filter is a combination of digital integrator and digital differentiator stages, which can perform the operation of digital low pass filtering and decimation at the same time.

Y. Djadi, *et al.* [2] designed a programmable decimation and interpolation digital filter based on the CIC structure. The circuit was configurable as either a decimation filter or an interpolation filter and the conversion ratio was programmable to any integer value from 10 to 256. The filter was designed with MOSIS 1.2 micron CMOSN standard cell libraries and data input rate could be as high as 50MHz. Alan Kwentus *et al.* [3] designed and fabricated a programmable CIC decimation filter in a 0.8 µm CMOS process whose decimation factor varied in power of two ranges of 2 to 1024. The integrator and comb stages were implemented using carry-save arithmetic in order to get high throughput. Kei-Yong Khoo et al [4] also presented an efficient architecture for the first carry-save integrator stage.

Hyuk Jun Oh and Yong H. Lee [5] used a simple interpolated second-order polynomial filter (ISOP) cascaded with a CIC decimation filter to effectively reduce the pass band distortion caused by CIC filtering with little degradation in aliasing attenuation.

Hong-Kui Yang and W. Martin Snelgrove [6] decomposed the decimation ratio R into two factors, namely,

R_1*R_2 (R_1 and R_2 are integers) to implementing a CIC decimation filter. Instead of using one CIC filter to decimate the high speed digital signal, they used two CIC decimation filters: one CIC filter with a decimation ratio of R_1, and one with a decimation ratio of R_2. The implementation of the first decimator was based on a polyphase decomposition.

Another way of implementation the CIC decimation filter was presented by Yonghong Gao *et al.* [7] in which the decimation factor N was constrained to an M-th power-of-two. The transfer function can be rewritten as the product of M identical low-order FIR filters. The sampling rate in this implementation decreased at every stage by a factor of two. The first stage was crucial to the throughput; the employment of parallel processing techniques enabled a higher clock rate. The polyphase decomposition technique used here is similar to that in reference.

Fred Harris *et.al.* [8] in 2008 proposed Simple multiplier free Sin based compensator with only two adders. The proposed method is computational efficient and less complex. G. J. Dolecek *et.al.* [9], [10] in 2009, designed a multiplierless CIC compensation filter based on the 2*M*-order filter and the sharpening technique. This technique attempts to improve the pass band and the stop band of a symmetric nonrecursive filter using the multiple copies of the same filter.

Recently in 2010, G. J. Dolecek *et. al.* [11], proposed an efficient technique to design a economical recursive generalized comb filters (GCFs). This technique quantizes the multipliers in the z-transfer function employing power-of-2 terms. G. Javanovic Dolecek *et. al.* [13] presented a efficient modification of the CIC cosine decimation filter in may 2010. The second order compensator filter is introduced at low rate in order to improve the passband. The coefficients of the compensator filter are presented in a canonical signed digits (CSD) form and can be implemented using only adders and shifts. Consequently, the resulting filter is a multiplierfree filter and exhibits a high attenuation in the stopband, as well as a low passband droop.

Multiplierless finite impulse response (FIR) filters are very attractive in VLSI (very large-scale integration) implementation. Most of the hardware complexity is due to multipliers, as filters require large number of multiplication, leading to excessive area, delay and power consumption even if implemented in a full-custom integrated circuits. Implementation of systems with multiplications may be simplified by using only a small number of shift and add operations.

In this paper we analyze the optimized performance of compensated CIC decimation filter with decimation factor 64 by minimizing the number of stages of integrator and comb (differentiator) to achieve hardware efficient and low power CIC decimation filter structure.

2. CASCADED INTEGRATOR COMB (CIC) FILTER

Cascaded integrator-comb (CIC), or Hogenauer filters, are multirate filters used for realizing large sample rate changes in digital systems. CIC filters are multiplierless structures, consisting of only adders and delay elements which is a great advantage when aiming at low power consumption. They are typically employed in applications that have a large excess sample rate. That is, the system sample rate is much larger than the bandwidth occupied by the signal. CIC filters are frequently used in digital down-converters (DDCs) and digital up-converters.

The CIC filter is a class of hardware-efficient linear phase finite impulse response (FIR) digital filters, consists of an equal number of stages of ideal integrator filters and comb filters. Its frequency response may be tuned by selecting the appropriate number of cascaded integrator and comb filter pairs. The highly symmetric structure of a CIC filter allows efficient implementation in hardware. However, the disadvantage of a CIC filter is that its pass band is not flat, which is undesirable in many applications. Fortunately, this problem can be alleviated by a compensation filter. CIC filters achieve sampling rate decrease (decimation) and sampling rate increase (interpolation) without using multipliers. The CIC filter first performs the averaging operation then follows it with the decimation. The transfer function of the CIC filter in z-domain is given in equation (4).

$$H[z] = H[z]_I^p . H[z]_C^p = \frac{\left(1-z^{-K}\right)^p}{\left(1-z^{-1}\right)^p} = \left(\frac{1-z^{-K}}{1-z^{-1}}\right)^p \qquad (1)$$

In equation (1), K is the oversampling ratio and p is the order of the filter. The numerator $(1–z^{-K})^p$ represents the transfer function of a differentiator and the denominator $1/(1– z_{-1})^p$ indicates the transfer function of an integrator. A simple block diagram of a first order CIC filter is shown in Figure 2. In a CIC filter, the integrators operate at high sampling frequency (f_s), and the comb filters operate at low frequency $\left(\frac{f_s}{K}\right)$. The clock divider circuit divides the oversampling clock signal by the oversampling ratio, K after the integrator stage. By operating the differentiator at lower frequencies, a reduction in the power consumption is achieved. To ensure high system clock frequencies, the CIC decimator is actually implemented using the pipelined architecture. The pipeline registers shorten the critical path through the differentiator cascade of the basic architecture.

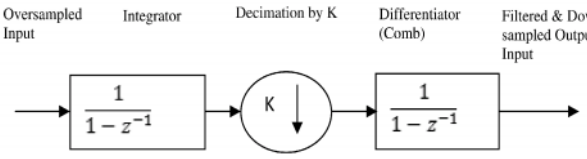


Figure 2: Block Diagram of First Order CIC Filter

3. DECIMATION TECHNIQUES

3.1. Using FIR Filters

The FIR Decimation block resamples the discrete-time input at a rate K times slower than the input sample rate. The block down samples the filtered data to a lower rate by discarding (K-1) consecutive samples following every sample retained. The design of FIR filter is based on the often added requirement that the phase response be linear. FIR filter is not based on any feedback path and can easily be designed to be linear phase by making the coefficient sequence symmetric i.e. equal delay at all frequencies. This property is sometimes desired for phase-sensitive applications. The structure of a FIR filter is given in Figure 1.

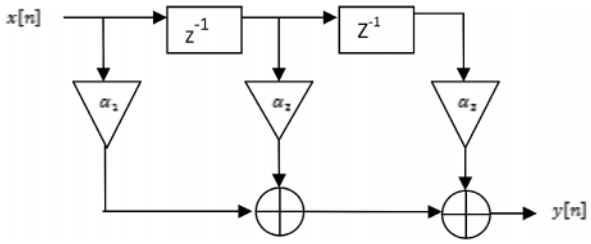


Figure 3: Structure of FIR Filter

The following figure shows the block diagram of such a 2nd-order moving-average filter:

$$h[n] = \alpha_1\delta[n] + \alpha_2\delta[n-1] + \alpha_3\delta[n-2] \qquad (2)$$

The main disadvantage of FIR filters is that considerably more computation power in a general purpose processor is required compared to an IIR filter with similar sharpness or selectivity, especially when low frequency (relative to the sample rate) cutoffs are needed. However many digital signal processors provide specialized hardware features to make FIR filters approximately as efficient as IIR for many applications.

3.2. Using IIR Filters

In multirate applications, the computational requirements for FIR filters can be reduced by the sampling rate conversion factor. However, such a degree of computation savings cannot be achieved in multirate implementations of IIR filters. This is due to the fact that every sample value computed in the recursive loop is needed for evaluating an output sample. Based on the polyphase decomposition, several techniques have been developed which improve the efficiency of IIR decimators and interpolators. Infinite impulse response (IIR) filters are used in applications where the computational efficiency is the highest priority. It is well known that an IIR filter transfer function is of a considerably lower order than the transfer function of an FIR equivalent. The drawbacks of an IIR filter are the nonlinear phase characteristic and sensitivity to quantization errors.

3.3. Using CIC Filters

These filters require no multipliers and use limited storage thereby leading to more economical hardware implementations. They are designated Cascaded Integrator-Comb (CIC) filters because their structure consists of an integrator section operating at the high sampling rate and a comb section operating at the low sampling rate. Using CIC filters, the amount of passband aliasing or imaging error can be brought within prescribed bounds by increasing the number of stages in the filter. However, the width of the passband and the frequency characteristics outside the passband are severely limited.

4. DIFFERENT COMPENSATION TECHNIQUES

When the number of stages is large, the CIC filter frequency response does not have a wide, flat pass band. To overcome the magnitude droop, a FIR filter that has a magnitude response that is the inverse of the CIC filter can be applied to achieve frequency response correction. Such filters are called “compensation filters.”

Several schemes have been proposed to design the compensation of CIC filter’s passband droop, mainly in the narrow pass band. The motivation behind the compensation methods is to appropriately modify the original CIC characteristic in the pass band such that the compensator filter has as low complexity as possible. Various methods used for compensation of CIC decimation filter are as follows:

4.1. CIC Roll-Off Compensation Filter

The CIC roll- off compensation filter is convolved with the channel selection filter. As the channel selection filter generally has the symmetric characteristics in frequency response, the CIC roll compensation filter should also have the symmetric characteristics. In this method, we compensates the roll off of the CIC filter in pass band by letting the CIC filter followed by a symmetric FIR filter with a minimum order. The coefficients of the compensation filter are given by- $\left[\frac{-v}{1-2v}, \frac{1}{1-2v}, \frac{-v}{1-2v}\right]$

The performance of the compensation filter depends on the value of v, which is obtained by minimizing the corresponding error function. CIC roll off compensation filter can be written as:

$$c(n) = \frac{-v}{1-2v}\delta(n+1) + \frac{1}{1-2v}\delta(n) + \frac{-v}{1-2v}\delta(n+1) \qquad (3)$$

And its frequency response $$C(w) = \frac{1-2v\cos w}{1-2v} \qquad (4)$$

Where, $v \neq 0.5$

$C(w)$ can work as a roll off compensation filter as it shows opposite frequency characteristics of CIC filter in

frequency domain. Let the frequency response of the CIC filter as F(ω) and the frequency response of an ideal filter as D(ω), then error function is defined by-

$$E_{uw(v)} = \int_0^{P_e} (D(w) - C(w) f(w))^2 dw \quad (5)$$

Where, P_e is pass band edge of the received signal. In general, it is difficult to define the exact pass band edge of the received signal due to the transition region in filter response. Therefore, the roll off phenomenon of the CIC filter can be exactly compensated if the frequency response characteristics of the received signal are used as a weighting function. In case of using the weighting function $W(w)$, the error function is given by-

$$E_{(v)} = \int_0^{\pi} (D(w) - C(w) f(w))^2 W(w) dw \quad (6)$$

Then, the error function $E(v)$ is minimized when the filter coefficient a is defined as:

$$v = \frac{\int_0^{\pi} f(w)(1 - coswf(w))\,(1 - f(w)W(w)dw}{\int_0^{\pi} f(w)(1 - coswf(w))(1 - cosw)W(w)dw} \quad (7)$$

It slightly improves the flatness of the pass band. This method focused on compensating the slope of the pass band, which is already fixed in the digital receiver, by letting the CIC filter followed by the compensation filter with a minimum computational load. It requires at least two multipliers. Better compensation in the wideband.

4.2. Compensated CIC-Cosine Decimation Filter

This method presents efficient modification of the CIC Cosine decimation filter. The second order compensator filter is introduced at low rate in order to improve the passband of interest of the overall filter. The coefficients of the compensator filter are presented in a canonical signed digits (CSD) form, and can be implemented using only adders and shifts. Consequently, the resulting filter is a multiplier free filter and exhibits a high attenuation in the stop band, as well as a low pass band droop.

Transfer function and magnitude response of compensation filter is given by-

$$H_{comp}\left(Z^M\right) = v + uz^{-M} + vz^{-2K} \quad (8)$$

$$\left|H_{comp}\left(e^{jKw}\right)\right| = |\,2v\cos(Kw) + u\,| \quad (9)$$

Where v & u real valued constant and K are is decimation factor.

Worst pass band distortion occurs at $w = 0$ & $w = w_c$ where $w_c = \frac{\pi}{KR}$ and R is the decimation factor of next decimation stage. In order to compensate the pass band droop at the frequency w_c then d_c should be less than 0.01 dB and 2 $cos(Mw_c) + b = \frac{1}{\delta_c}$. v and u can be calculate by-

$$\begin{bmatrix} v \\ u \end{bmatrix} = \begin{bmatrix} \frac{-1}{2(\cos(Kw_c)-1} & \frac{1}{2(\cos(Kw_c)-1} \\ \frac{\cos(Kw_c)}{(\cos(Kw_c)-1} & \frac{-1}{(\cos(Kw_c)-1} \end{bmatrix} \begin{bmatrix} 1 \\ \delta_{comp} \end{bmatrix} \quad (10)$$

Where $\delta_{comp} = \frac{1}{\delta_c}$ and If the pass band droop is within the desired limit then the magnitude response can be presented in canonical signed digit (CSD).

$$H_{comp-CSM}(Z^K) = v_{CSD} + u_{CSD}Z^{-K} + v_{CSD}Z^{-2K} \quad (11)$$

Where v_{CSD} and u_{CSD} are the CSD representations of the quantized coefficients of the coefficient of compensation filter. The procedure is continued until the desired Pass band compensation is obtained. There is a trade off between the desired compensation of the pass band droop and filter coefficients can control the desired pass band droop of the overall decimation filter.

5. ANALYSIS AND FREQUENCY RESPONSES

5.1. CIC Cascaded with FIR Filter Sections: Delay = 1, Sections = 1

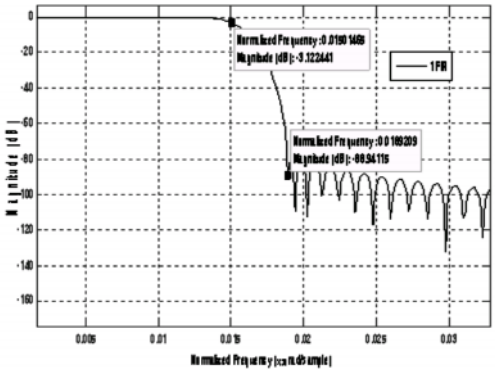
Stages	*Decimation Ratios (64)*	*Cut off frequencie π rad/sample*	*Gain (DB)*
1 FIR, 1 CIC	8, 8	0.015	18.1
1 FIR, 2 CIC	4, (8,2)	0.027	24.1
2 FIR, 2 CIC	(4,2), (4,2)	0.029	18.1
3 FIR, 1 CIC	(4,2,4), 2	0.016	6
2 FIR, 1 CIC	(8,4), 2	0.0165	6

5.2. CIC Compensator Analysis Table: Delay = 1

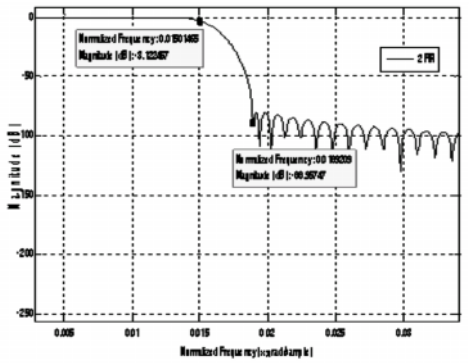
CIC Sections	*F pass*	*F stop*
1	0.4741	0.5529
2	0.4783	0.5515
3	0.4812	0.5506

5.3. Frequency Responses

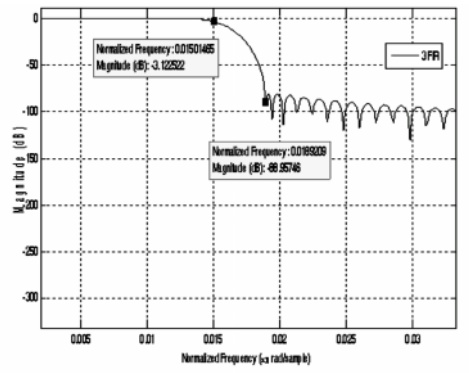
(a) FIR Filter stages with decimation ratio 64



(a) Single FIR Stage



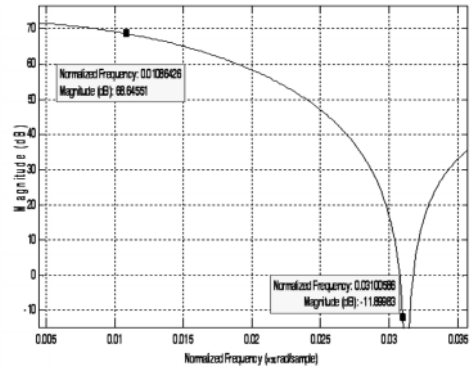
(b) Two FIR Stage



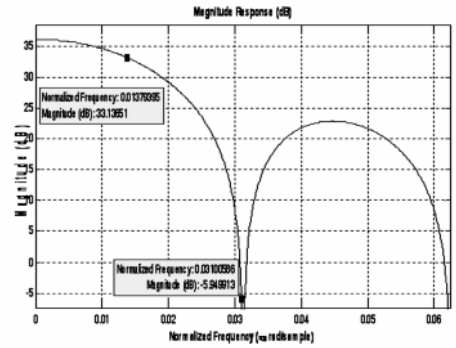
(c) Three FIR Stage

Figure 5

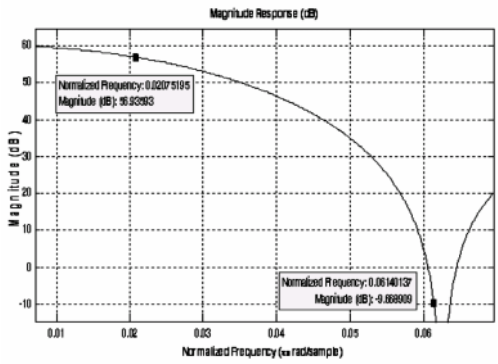
(b) CIC Filter stages with decimation ratio 64



(a) Single CIC Stage



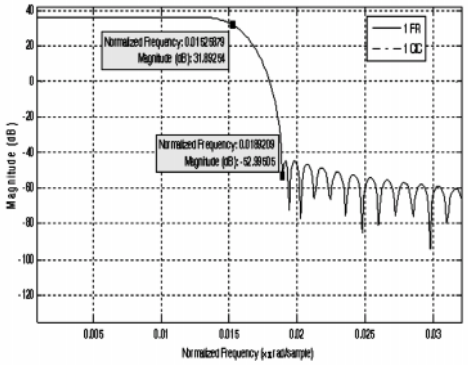
(b) Two CIC Stage



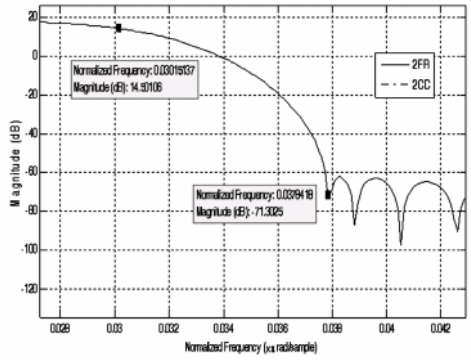
(c) Three CIC Stage

Figure 6

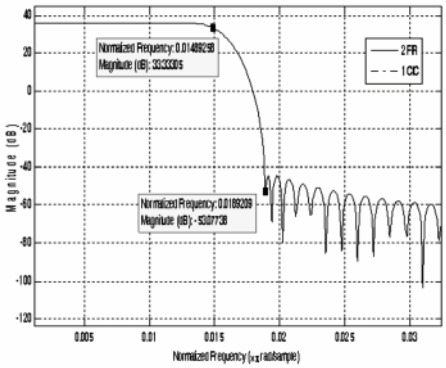
(c) Compensated CIC Filter with decimation ratio 64



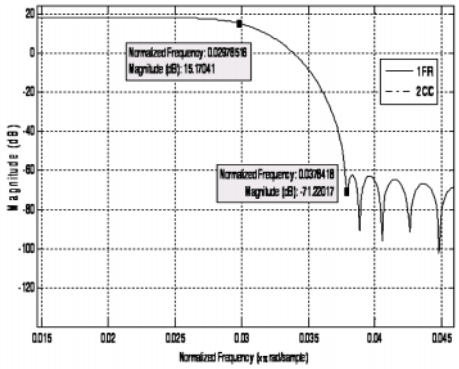
(a) One CIC Filter with One FIR Filters (8X8)



(b) Two CIC Filter with Two FIR Filters (4,2)X(4,2)



(c) One CIC Filter with two FIR Filters with K= 8X(4,2)



(d) Two CIC Filters with One FIR Filter with K= (8,2)X4

Figure 7

6. CONCLUSION

Decimation of a signal at high frequency using FIR or IIR structures is very complex since it needs a lot of multiplications and hence system cost is increased. In CIC filter as the number of stages increases its stop band attenuation improves but pass band droop increases. In many applications monotonically decreasing pass band droop has to be compensated. CIC filters are very economic, computationally efficient and simple to implement in comparison with FIR or IIR for large rate change due to lack of multipliers. One of the difficulties in using CIC filters is accommodating large data word growth, particularly when implementing integrators in multistage CIC filters. This paper analyzed the performance of CIC decimation filter for efficient compensation by using CIC filter as a first stage in decimation when the overall decimation factor is factorized. For overall decimation factor of 64, a sampling rate conversion system is analyzed by cascading different stages of CIC and FIR filters and found that CIC filter with large sampling rate improves the stop band attenuation whereas the FIR filters provide the desired passband transition characteristics. This paper also analyzed the single and multistage CIC decimation filters for decimation ratio 64 for efficient compensation of passband droop.

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