IJEE 0973-7383 Volume-8 • Number-2 Jun -Dec 2016 pp. 32-35 available online at www.csjournalss.com

Static VAR Compensation using Multilevel Inverter

[1]K.Arunkumaran [2]D.Jayaraj
[1-2]Assistant Professor ,Department of Electrical and Electronics Engineering,
M.I.E.T. Engineering College, Trichy

Abstract

Now a days supplying high quality power to the critical loads like medical equipment, research instruments etc is a vital importance. Different hardware structure and techniques have been applied to obtain a pure supply. The distortion of the output voltage decreases as the number of level increases and it is further improved by applying pulse width modulation (PWM) techniques. In this work an attempt is made to reduce the harmonic content in the output voltage by incorporating a single phase nine level cascaded multi level inverter and PWM techniques. This work presents harmonic analysis of single phase nine level cascaded type multilevel inverter. The gating signals for the switches are generated with the help of the switching table. Using various PWM techniques the power circuit is simulated in MATLAB Simulink package and the simulation results are presented. A comparative analysis is made for various values of switching angles and an equal input dc supply. Voltage sags are one of the most dominating power quality assets, which dragged the attention of many researchers as the sensitivity of loads are increasing due extensive usage of power electronic devices. Fault at distribution level, sudden increase of loads, motor starting are some of the causes of the voltage sags. Such sudden variations of voltage are undesirable for sensitive loads. These undesirable voltage sags can be mitigated by connecting controlled devices either in series or shunt to the load. A few of such devices are dynamic voltage restorer (DVR) and STATCOM . Both these devices require voltage source converters to satisfactory operation .

Keywords:

Multilevel inverter, Harmonics, Total Harmonic Distortion (THD), Low Order Harmonics (LOH), Pulse Width Modulation (PWM)

Introduction

Increasing attention has been paid to multilevel dc/ac inverters in recent years to obtain output voltage of high quality . Various modulation methods have been developed for multilevel inverters. A very popular method in industrial applications is the classic carrier-based sinusoidal pulse width modulation (SPWM) that uses the phase shifting technique to reduce harmonics in the load voltage . In SPWM, the states of power semiconductor switches are determined by the comparison of reference signals and saw tooth signals. Another important modulation method for multilevel inverters is the optimal PWM, which includes step modulation , multilevel selective harmonic elimination and optimal combination modulation. With the same switching frequency, voltage quality generated by the optimal PWM is better than that by the popular SPWM or the space vector PWM. The general procedure for implementing optimal PWM is based on Fourier series analysis.

Generally, the equation sets are nonlinear and transcendental. These equations can be solved by any iterative method. The THD of the output voltage of the inverter is a measurement of the harmonic distortion, which is expected to be as small as possible in many applications of multilevel inverters.

Cascaded Multilevel Inverter

Structure of Single Phase Nine Level Cascaded Multilevel Inverter

Among three types of topologies of multi-level inverter (Diode-clamped multilevel inverter, Flying capacitors multilevel inverter, cascaded multilevel inverter), the cascaded type is considered for this work because of simple structure. The structure of single phase cascaded nine level Inverter is shown in figure 1. Each bridge is energized by separate DC sources which may be obtained from batteries, fuel cells, solar cells or ultra capacitors. The number of levels in output voltage of a cascaded multi-level inverter is ,where S is the number of dc sources .

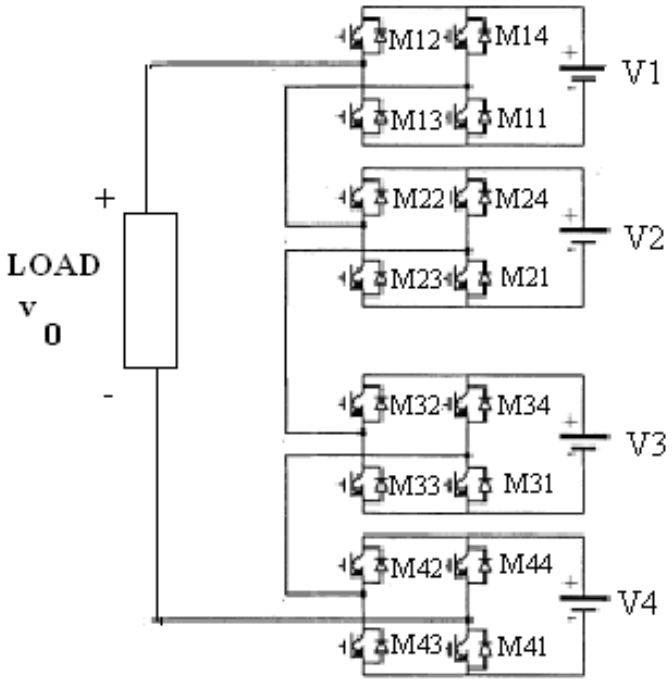


Figure 1: Structure of single phase cascaded nine level inverter

A descriptive voltage waveform for a nine level cascaded inverter is shown in Figure 2. The maximum output voltage is given by

V0 = V1+V2+V3+V4.

With enough levels and an appropriate switching algorithm, the multilevel inverter results in an output voltage that is near sinusoidal.

Method of Working

The output voltage of the nine level cascaded multi-level Inverter is shown in figure 2. The steps to synthesize the nine level voltages are as follows .

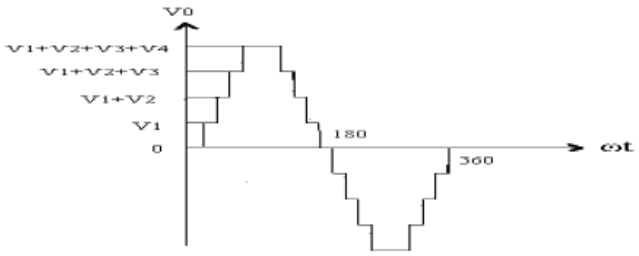


Figure 2: Output voltage of single phase cascaded nine level inverter

1. For an output voltage level V0 = V1, the switches M11, M12, M22, M32 and M42 are turned on.
2. For an output voltage level V0 = V1+V2, all the switches as mentioned in step 1 and M21 are turned on.
3. For an output voltage level V0 = V1+V2+V3, all the switches as mentioned in step 2 and M31 are made on.
4. For an output voltage level V0 = V1+V2+V3+V4, all the switches as mentioned in step 3 and M41 are kept on.

Switching Table For Nine Level Cascaded Multilevel Inverter

Table 1 shows the voltage levels and their corresponding switch states for the positive half cycle of the output voltage. State condition 1 means the switch is on and 0 means the switch is off. Each switch is turned on only once per cycle and therefore reduces switching losses.

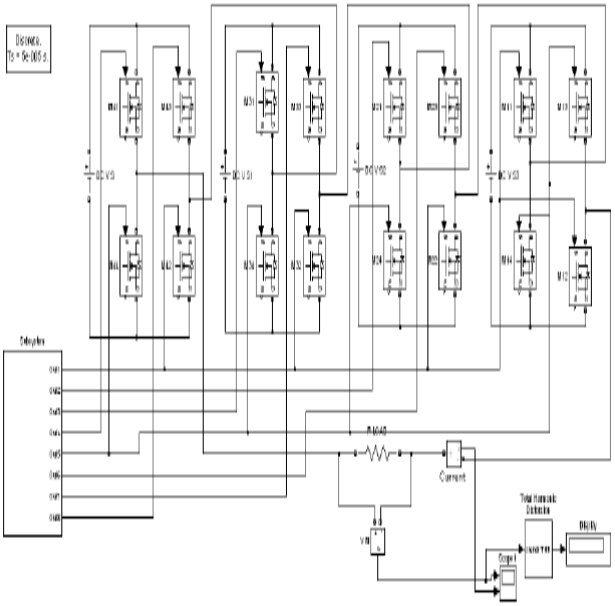
Table 1: Output voltages and their corresponding switching states

SWITCHES	OUTPUT VOLTAGAE V_0			
	V1	V1+V2	V1+V2+V3	V1+V2+V3+V4
M_{11}	1	1	1	1
M_{12}	1	1	1	1
M_{13}	0	0	0	0
M_{14}	0	0	0	0
M_{21}	0	1	1	1
M_{22}	1	1	1	1
M_{23}	0	0	0	0
M_{24}	0	0	0	0
M_{31}	0	0	1	1
M_{32}	1	1	1	1
M_{33}	0	0	0	0
M_{34}	0	0	0	0
M_{41}	0	0	0	1
M_{42}	1	1	1	1
M_{43}	0	0	0	0
M_{44}	0	0	0	0

Simulation Results

Simulation of Cascaded Multilevel Inverter

The Simulink model of the proposed nine level cascaded multilevel inverter system for various PWM techniques is shown in figure 3. This circuit comprises four single phase bridges connected in cascade and MOSFET switches are used. Four separate voltage sources of value Vdc=90V is used to energize the power circuit. The load on the inverter is resistive of value R= 50 ohms. Simulation of power circuit is carried out using control circuit which generates required gating signals. Three different PWM techniques are used to produce the gating signals. Using this signal, the output voltage and current waveforms are obtained and the corresponding frequency spectrum is also analyzed.



Simulink model for nine-level cascaded multilevel inverter system

Single Pulse Width Modulation Technique

In this technique, single pulse is produced in each half cycle for various switches as per their requirements in order to obtain nine level output voltage and current. Figure 4 shows the control circuit of the nine level multilevel inverter. A triangular carrier wave is compared with a shifted dc levels to have pulses for various switches. The circuit is simulated in MATLAB and the corresponding switching signals are shown in figure 5.

The power circuit is simulated in MATLAB-Simulink package with the use of gating signals generated in the figure 5. The output voltage and current waveform are shown in figure 6. Since the load is resistive, the current is in-phase with the output voltage. The corresponding frequency spectrum of the output voltage is shown in figure-7. The total harmonic distortion for the waveform shown in figure 6 is 21.64%.

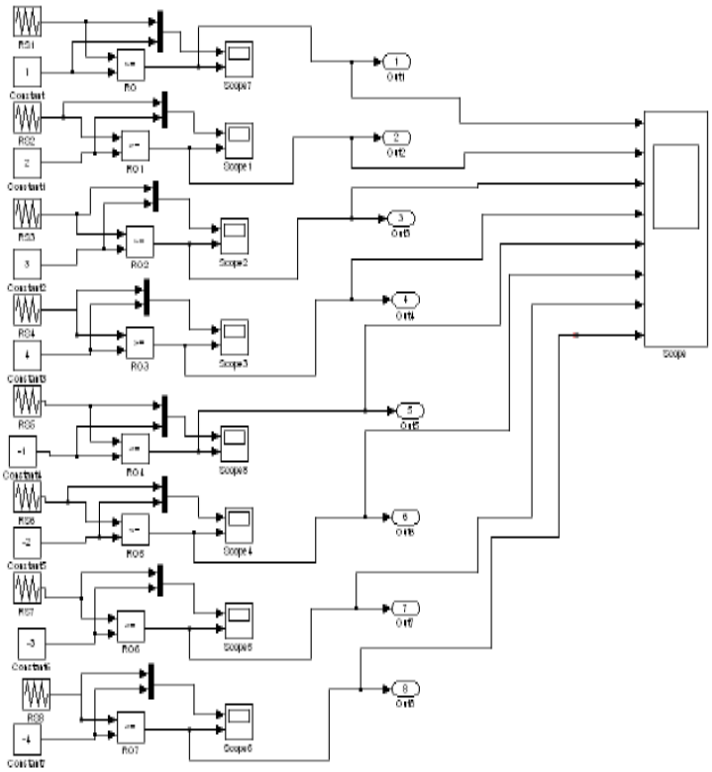


Figure 4: Simulink model of the gating pulse generation for Single PWM

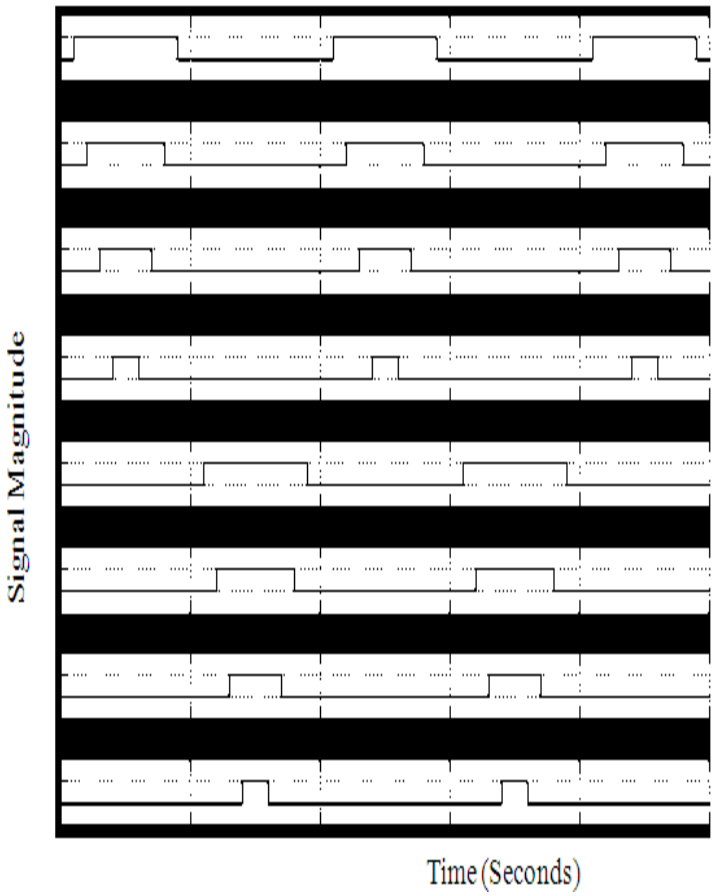


Figure 5: Gating pulses for various switches in Single PWM

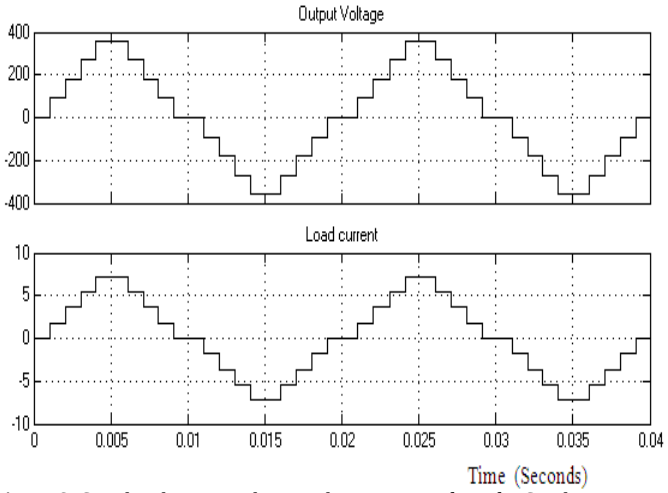


Figure 6: Simulated output voltage and current waveform for Single PWM

Sinusoidal Pulse Width Modulation Technique

In this technique fundamental frequency sinusoidal waveform is compared with high frequency triangular wave. For the particular range of reference voltage the modulation index (M) is varied. Since the shifted triangular waveform is necessary for the desired gating signal the modulation index range is restricted to 0.775 to 1.The simulation is done using the switching signals shown in figure 7 for the particular range of modulation index (M) and the corresponding output voltage is obtained. The output voltage and frequency spectrum of it for the case of sinusoidal PWM technique are shown in the figures 8. The total harmonic distortion for the output waveform shown in figure 13 is 11.95%. Figure 14 shows harmonic profile of SPWM based circuit in which the magnitude of lower order harmonics is less compared with higher order harmonics.

Figure 7: Gating pulses for various switches in sine PWM

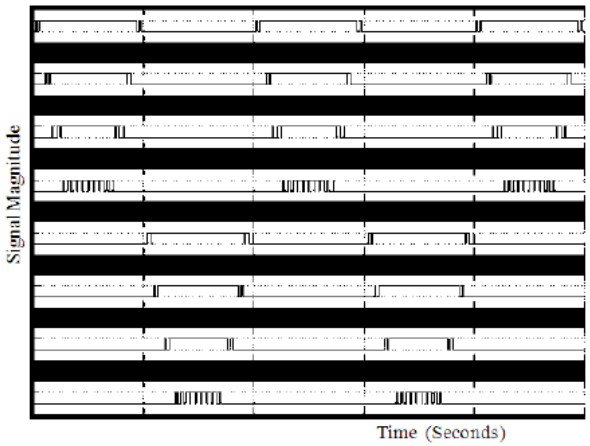
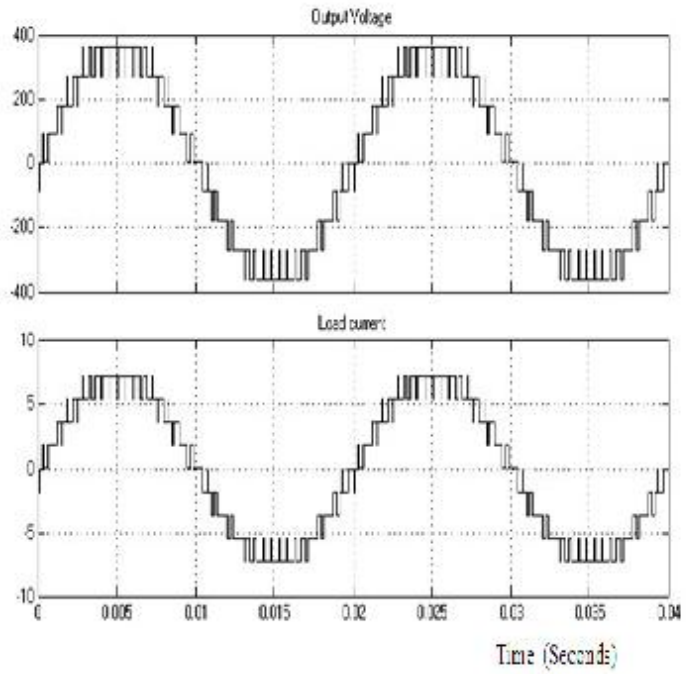


Figure 8: Simulated Output voltage and current waveform for sine PWM



Conclusion

A single phase nine-level cascaded multilevel inverter has been simulated with different PWM techniques and the quality of its output voltage is analyzed. The simulation has been carried out for different set of switching angles, maintaining supply voltage equal and constant. The simulation results show that THD values for single, multiple and sinusoidal PWM. The sinusoidal PWM techniques are useful in eliminating lower order harmonics. The higher order harmonics can be easily eliminated by filters. Hence it is observed that the sinusoidal PWM technique gives better results compared to other PWM techniques. Further optimization techniques may be introduced to have lowest THD.

References

[1] J. Rodriguez, J. S. Lai, and F. Z. Peng, "Multilevel inverters: A survey of topologies, controls, and applications," *IEEE Trans. Ind. Electron.*, vol. 49, no. 4, pp. 724–738, Aug. 2002.

2] V. G. Agelidis, A. Balouktsis, I. alouktsis,andC.Cossar,"Multiple sets of solutions for harmonic elimination PWM bipolar waveforms: Analysis and experimental verification," *IEEE Trans. Power Electron.*, vol. 21, no. 2, pp. 415–421, Mar. 2006.

[3] X. Xu, Y. Zou, K. Ding, and F. Liu, "Cascade multilevel inverter with phase-shift SPWM and its application in STATCOM," in *Proc. IEEE IECON*, 2004, vol. 2, pp. 1139–1143.

[4] Y. Ikeda, J. Itsumi, and H. Funato, "The power loss of the PWM voltage-fed inverter," in *Conf. Rec. IEEE PESC'88*, 1988, pp. 277–283.

[5] P. M Ehagwat and V. R stefanovic, "Generalized structure of a multilevel inverter," *IEEE Trans. Ind Applicat.*, vol 19, no 6, pp. 1057-1069, Nov./Dec. 1983.

[6] R. Lund, M. Manjrekar, P. Steimer, and T. Lipo, "Control strategy for a hybrid seven-level inverter," in *Proc. European Power Electronics Conf.(EPE'99)*, Lausanne, Switzerland, 1999, CD-ROM.

7] S. Sirisukprasert, J.-S. Lai, and T.-H. Liu, "Optimum harmonic reduction with a wide range of modulation indices for multilevel converters," *IEEE Trans. Ind. Electron.*, vol. 49, no. 4, pp.875– 881, Aug. 2002.

[8] L. Tolbert and T. G. Habetler, "Novel multilevel inverter carrier-based PWM method," *IEEE Trans. Ind. Applicat.*, vol. 35, pp. 1098–1107, Sept./Oct. 1999.

[9] H. S. Patel and R. G. Hoft, "Generalized harmonic elimination and voltage control in thyristor inverters: Part I—Harmonic elimination," *IEEE Trans. Ind. Applicat.*, vol. 9, no. 3, pp. 310–317, May/Jun. 1973.

[10] V. G. Agelidis and M. Calais, "Application specific harmonic performance evaluation of multicarrier PWM techniques," in *Proc. IEEE PESC'98*, Fukuoka, Japan, May 1998, pp. 172–178.

[11] P. Enjeti and J. F. Lindsay, "Solving nonlinear equations of harmonic elimination PWM in power control," *IEE Electronics Letters*, vol 23, no. 12, June 4, 1987, pp 656-657.