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Oscillation-Based Test Technique for Analog Cores in Mixed-Signal Integrated Circuits Using the Field Programmable Analog Array Technology

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Abstract: Modern System-on-Chip (SoC) designs are increasingly mixed-signal Very Large Scale Integrated (VLSI) designs that require efficient design and testing methodologies to manage the design complexity and the time-to-market constraints. Also, in mixed-signal integrated circuits (ICs), testing analog cores is the most difficult task and it's one of the major cost factors in the overall IC manufacturing cost. Hence, developing testing approaches that reduce the test cost and accelerate the time-to-market is too challenging. This paper presents an oscillation based test technique implemented using the Field-Programmable Analog Array (FPAA) technology. In fact, using the proposed approach we will distinguish a faulty circuit from a fault-free one by controlling the oscillation frequency of the Circuit under Test (CUT). Actually, faults that occur in the CUT can be detected by checking whether the oscillation frequency has deviated from its nominal value. The system is practically designed and simulated by using the AN221E04 board which is an Anadigm product. The circuit validation was carried out using the AnadigmDesigner®2 software. Simulation results show that the proposed testing technique is effective and can be used to reduce the design and testing costs of mixed-signal ICs.

Keywords: Mixed-signal ICs, design, test, FPAA, Oscillation frequency.

1. INTRODUCTION

In the digital domain, digital circuit designs are quickly validated on a computer with the help of well-developed and commercially available CAD tools [1]. In addition, Programmable Logic Devices (PLDs) have a large impact on the development of custom digital chips by enabling the designer to try custom designs on easily-reconfigurable hardware. In fact, since their conception in the late 1960s, PLDs have evolved into today's high-density Field Programmable Gate Arrays (FPGAs) which overcome the use of Application-Specific Integrated Circuits (ASICs) in today's digital system design [2]. On the other side, unlike digital circuits which are based on two binary states, analog circuits deal with an infinite range of values. Also, the performance of analog designs is sensitive to any small variation occurring during the manufacturing process. In addition, the severe impact of noise and leakage currents, the influence of external magnetic fields and the interaction with other components makes analog ICs harder to design. In fact, despite the great progress achieved in the past few years concerning analog circuit technologies, analog design tools are still far from reaching a mature stage. Even today there are not CAD tools that can guarantee the success of analog IC designs [3]. Thus, with the continuous increase of integration densities and complexities, the tedious and hard process of designing and implementing analog ICs could often take weeks or even months [2]. However, the evolutionary trend in VLSI circuits technologies fuelled by fierce industrial competition to reduce ICs cost and time to market has led to design the FPAA which is the analog equivalent of the FPGA. In fact, the use of FPAAs reduces the complexity of analog ICs design and testing, decreases the time to market and allows products to be easily updated and improved outside the manufacturing environment [4].

Thus, the current paper presents an oscillation based test technique for Analog Cores in Mixed-Signal ICs using the Field Programmable Analog Array Technology. The proposed testing strategy is based on transforming the circuit under test (CUT) into a sinusoidal oscillator and then measuring the oscillation frequency, therefore the deviation of the oscillation frequency from its nominal value can be used to detect the presence of faults in the CUT.

The paper is organised as follows. In section 2, we introduce the FPAA technology. We then present The AN221E04 Anadigm board in section 3. The proposed oscillation based test technique using the FPAA technology is presented in sections 4 and 5. The simulation results are illustrated in section 6. Finally, we conclude in section 7.

2. THE FPAA TECHNOLOGY DESCRIPTION

Reconfigurable analog hardware has been progressing much more slowly than their digital analogues. In fact, the FPAA technology appeared in 1980's [5-6] while the commercial FPAA did not reach the market until 1996 [2] and the Anadigm FPAA technology was made commercially

available only in 2000 [7]. Actually, the FPAAs provide a method for rapidly prototyping analog systems. The currently available commercial and academic FPAAs are built in Complementary Metal Oxide Semiconductor (CMOS) technology. In this paper, we focus on Anadigm's FPAA family based on switched capacitor technology. The most important element in the FPAA is the Configurable Analogue Block (CAB), which is analogous to the Computational Logic Block (CLB) found in FPGAs. A CAB includes an operational amplifier and manipulates a network of switched capacitor technology. Using the AnadigmDesigner®2 software and its library of analog circuit functions, a designer can easily and rapidly design a circuit that would previously have taken months to design and test. The circuit configuration files are downloaded into the FPAA circuit from a PC or system controller or from an attached EEPROM [4-8]. Modern FPAAs like Anadigm products contain analog-to-digital converters that make them suitable for integration with complex, digital-signal-processing, FPGA and microcontroller blocks [2]. In the next section we present the Anadigm® AN221E04 FPAA device which is based on switched capacitor technology [8].

3. THE AN221E04 ARCHITECTURE

The AN221E04 device consists of a 2x2 matrix of fully Configurable Analog Blocks, surrounded by programmable interconnect resources and analog input/output cells with active elements. Configuration data is stored in an on-chip SRAM configuration memory. The AN221E04 device features six input/output cells. In fact, The AN221E04 devices have four configurable I/O cells and two dedicated output cells [4-8]. The architectural overview of the AN221E04 device is given by Figure 1.

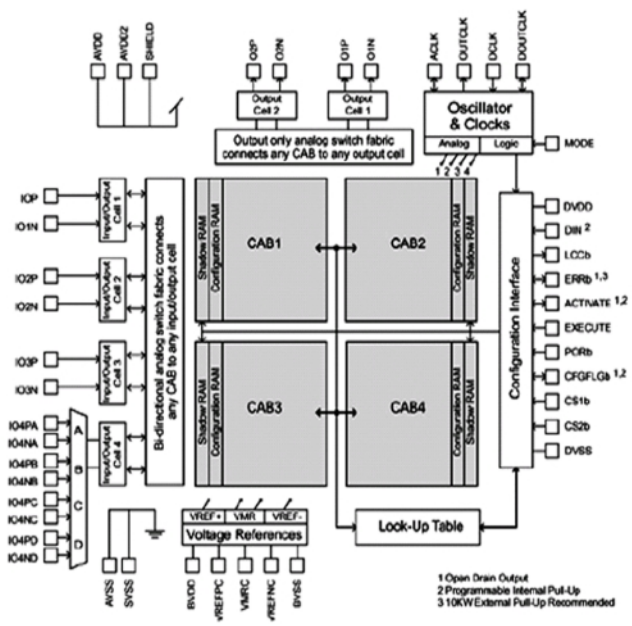

Figure 1: Architectural Overview of the AN221E04 Device [8]

The circuit design is enabled using AnadigmDesigner®2 software, which includes a large library of analog circuit functions such as gain, summing, filtering, etc.. These circuit functions are represented as CAMs (Configurable Analog Modules) which are configurable blocks mapped onto portions of CABs. The circuit implementation is established through a serial interface on the AN221E04 evaluation board using the AnadigmDesigner®2 software, which includes a circuit simulator and a programming device. A single AN221E04 can thus be programmed and reprogrammed to implement multiple analog functions [4-8].

4. THE OSCILLATION BASED TEST TECHNIQUE FOR TESTING ANALOG CORES IN MIXED-SIGNAL ICS USING THE FPAA TECHNOLOGY

4.1. Testing Analog Cores in Mixed-signal Integrated Circuits

The continuous growth of integration densities in CMOS technology has led to design and manufacture very complex mixed-signal ICs including digital, analog and mixed circuits in the same chip, this approach is known as system-on-a chip approach design [9-10-11]. For mixed-signal ICs, analog circuits coexist with digital components. Thus, testing difficulties increase considerably because the access to both analog and digital blocks is severely restricted [12]. Thus, there are many problems with analog circuits testing such as the node accessibility problems and the lack of common test strategies and standards. Consequently, analog designers are faced with many new challenges at different phases of design and testing of mixed-signal ICs. So, test approaches and techniques for analog and mixed signal blocks are gaining importance [13-14].

4.2. The Proposed Testing Technique Description

This work presents a test method for testing analog ICs by measuring the oscillation frequency deviation of a CUT from a center nominal frequency. Therefore, during the test mode, faults in the CUT that cause a reasonable deviation of the oscillation frequency from its nominal value can be detected. The proposed testing technique can be applied to electronic oscillator circuits that produce a repetitive electronic signal. Common examples of signals generated by oscillators include signals broadcast by radio and television transmitters and clock signals that regulate computers and quartz clocks. Also, this testing approach is not restricted only on electronic oscillator circuits since analog circuits under test can be easily converted into a circuit that oscillates. This testing technique is well-known in literature as Oscillation-Based Test technique (OBT) [12]. In fact, the basic idea is to transform the CUT into a sinusoidal oscillator and to measure the oscillation frequency to alert on potential faults. Theoretically, converting any analog system into an oscillator consists in adding a feedback path to the circuit structure and then regulating the feedback elements until

obtaining oscillation. Figure 2 illustrates a CUT converted into an oscillator [12].

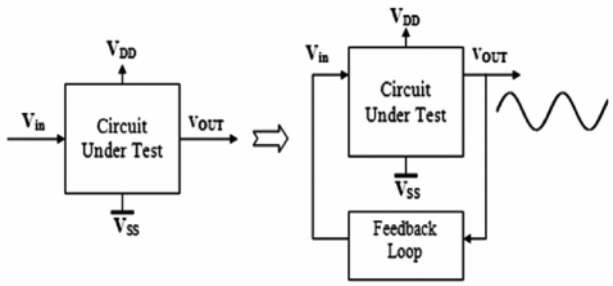

Figure 2: A Circuit Under Test Converted into an Oscillator [12]

"Such an oscillator inertly produces a test signal whose oscillation frequency depends on the fault-free structure of the CUT in such a way that its predicted value can be considered as a test-signature. So, faults that occur in the CUT can be detected by checking whether the oscillation frequency has deviated from its expected nominal value. In this testing approach, two modes have to be distinguished: an operational mode when the system is connected to its regular input and all the additional components required for testing are removed, and a test mode where the feedback loop is closed around the CUT, its regular input is disconnected, and potentially some circuitry is removed and/ or added in the CUT for test purpose" [12].

5. THE PROPOSED TESTING METHODOLOGY USING THE FPAA TECHNOLOGY

The proposed testing strategy is based on controlling the oscillation frequency of the circuit under test which can be already an electronic oscillator circuit or it can be an analog circuit converted into an oscillator. The most important in this oscillation based test technique is that the nominal oscillation can be accurately modelled and can be used as a test signature. The Oscillation-frequency based testing approach is illustrated in Figure 3.

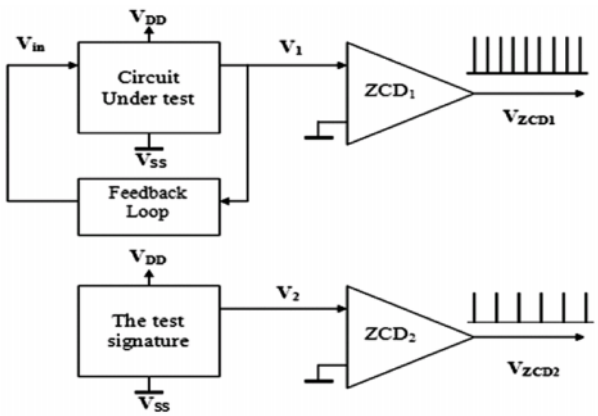

Figure 3: The Bloc Diagram Illustrating the Proposed Testing Approach

In Figure 3, V_1 and V_2 are respectively the output of the analog CUT converted into an oscillator and the test signature which is the fault-free output of the CUT that oscillates at a nominal oscillation frequency (f_{REF}). ZCD_1 and ZCD_2 are two zero crossing detector circuits. In fact each zero crossing detector circuit produces a pulse when the input changes from negative to positive. The current testing approach is based on counting the pulses generated using the two zero crossing detector circuits during the time devoted to test. N_{CUT} is the number of pulses generated using the first zero crossing detector circuit (ZCD_1) during the time devoted to test while N_{REF} is the number of pulses generated using the second zero crossing detector circuit (ZCD_2) during the time devoted to test. Thus, the circuit under test oscillation frequency (f_{CUT}) and the oscillation frequency deviation (f_D) can be expressed as:

$$\begin{cases} f_{CUT} = f_{REF} \times \dfrac{N_{CUT}}{N_{REF}} \end{cases} \quad (1)$$

$$\begin{cases} f_D = f_{REF} \times \dfrac{(N_{CUT} - N_{REF})}{N_{REF}} \end{cases} \quad (2)$$

In the next section we will implement the oscillation based test circuit using the AN221E04 board which is an Anadigm FPAA product. The general test procedure is presented in Figure 4.

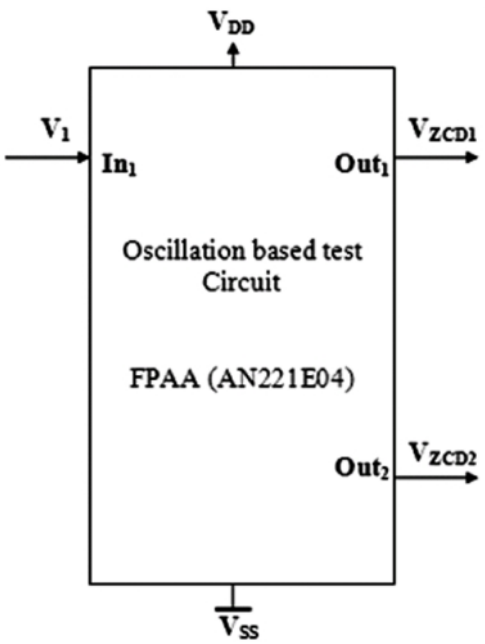

Figure 4: The Proposed Test Approach Using the AN221E04 FPAA Device

In Figure 4, we can notice that V_1, which is the output of the analog CUT converted into an oscillator, is the only input used in the oscillation based test circuit configured

using the AN221E04 board. Thus, there is no hardware redundancy needed in this testing approach because the fault-free oscillation is perfectly generated by adjusting the parameter of the Sine Wave Oscillator CAM provided by the FPAA. Actually, V_1 must to be connected to the first zero crossing detector CAM in order to obtain the first output V_{ZCD1} while the test signature, which is the fault-free oscillation generated by the sine wave CAM inside the FPAA, is connected to the second zero crossing detector CAM in order to obtain the second output V_{ZCD2}. The Circuit design and implementation are enabled using AnadigmDesigner®2 software. The circuit design illustrating our test methodology is presented in Figure 5.

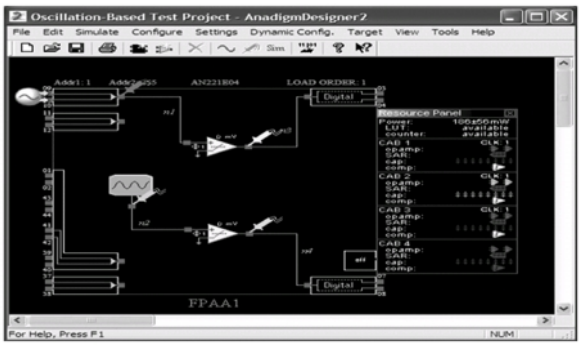

Figure 5: The Oscillation Based Test Circuit Implemented Using the AN221E04 FPAA Device

From Figure 5, we note that the oscillation based test circuit implementation only needs the use of three CAMs which are two zero crossing detector circuits (ZCD_1 and ZCD_2) and the Sine Wave Oscillator CAM that generates the test signature (V2). As shown in the resource panel illustrated in the same figure the circuit implementation requires the use of three CABs (CAB 1, 2 and 3).

6. SIMULATION RESULTS

Figure 6 illustrates the simulation results of the implemented oscillation based test circuit using a fault-free CUT.

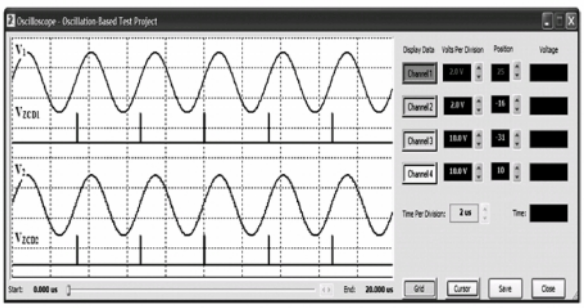

Figure 6: The Oscillation Based Test Circuit Waveforms

During the time devoted to test, which is equal to 200 µs, the two signals V_{ZCD1} and V_{ZCD2} presents the same number of pulses ($N_{CUT} = N_{REF} = 59$). Thus, the oscillation frequency of the CUT is equal to the nominal frequency of the test signature ($f_{CUT} = f_{REF}$=300 KHz) while the deviation of the oscillation frequency is equal to 0 (f_D=0 KHz). In fact, these results are quite normal because they corresponds on the fault-free CUT simulation results. Figure 7 (a) and (b) illustrate the waveforms of the oscillation based test circuit obtained by simulating a faulty circuit under test that oscillates at a frequency equal to 310 KHz ($f_{CUT} > f_{REF}$).

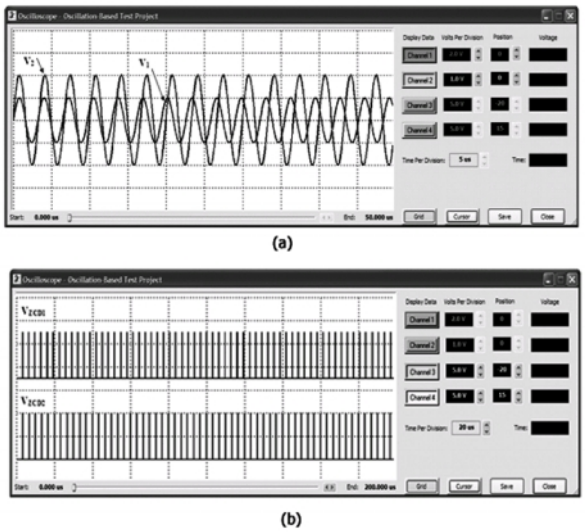

Figure 7: The Oscillation Based Test Circuit Waveforms Obtained by Simulating a Faulty CUT

As illustrated in Figure 7 (b), during the time devoted to test, which is equal to 200 µs, the two signals V_{ZCD1} and V_{ZCD2} presents different number of pulses (N_{CUT} =61 and N_{REF} = 59). Thus, the oscillation frequency of the CUT is equal to 310, 16 KHz (f_{CUT}=300*61/59=310,16 KHz) while the deviation of the oscillation frequency is equal to 10,16 KHz (f_D= 300*(61-59)/59= 10,16 KHz). Hence, simulation results shown by Figure 7 ensure that the oscillation based test circuit behaves as intended. In fact, the oscillation frequency deviation indicates that the oscillation frequency has deviated from its expected nominal value. Therefore we assume that the CUT is faulty and we precede to the correctness acts.

Figure 8 illustrates the waveforms of the oscillation based test circuit obtained by simulating a faulty CUT that oscillates at a frequency equal to 250 KHz ($f_{CUT} < f_{REF}$).

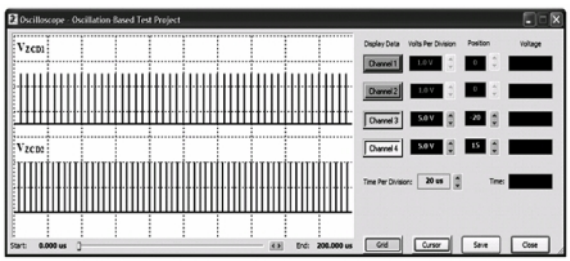

Figure 8: Output of the Oscillation Based Test Circuit Obtained by Simulating a Faulty CUT

During the time devoted to test, which is equal to 200 µs, the two signals V_{ZCD1} and V_{ZCD2} presents different number of pulses (N_{CUT} =49 and N_{REF} = 59). Thus, the oscillation frequency of the CUT is equal to 249,15 KHz (f_{CUT}=300*49/59=249,15 KHz) while the deviation of the 0oscillation frequency is equal to -50,84 KHz (f_D= 300* (49-59)/59=-50,84 KHz). Hence, simulation results shown by Figure 8 ensure that the oscillation based test circuit behaves as intended. In fact, the oscillation frequency deviation indicates that the oscillation frequency has deviated from its expected nominal value which proves that the CUT is faulty.

Thereby, simulation results prove the validity of the proposed test method. In addition, using this test technique, no test vector is required to be applied. Therefore, the test vector generation problem is eliminated while the test time is very small. These characteristics imply that the proposed test strategy is very attractive for wafer-probe testing as well as final production testing.

7. CONCLUSION

This paper presented a testing technique based on controlling the oscillation frequency of the circuit under test which can be already an electronic oscillator circuit or it can be an analog circuit converted into an oscillator. The proposed technique is used to detect faults in the CUT by checking if the oscillation frequency deviates from its nominal value. The proposed approach is implemented using the Field Programmable Analog Arrays technology which introduces new opportunities to improve analog circuit design and testing by providing a method for analog systems rapid prototyping. Simulation results show that the technique is effective and prove that the analog integrated circuit design and testing become easier using the Field Programmable Analog Array technology.

References

[1] G. Gielen and R. Rutenbar, Computer-Aided Design of Analog and Mixed-signal Integrated Circuits, Proceedings of the IEEE, Volume 88, Issue 12, pp. 1825-1854, December 2000.

[2] P. Hasler, Tyson S. Hall, and CM. Twig, Large-scale Field-programmable Analog Array, Institute of Neuromorphic Engineering Publication, 2005.

[3] Manuel F. M. Barros, Jorge M. C. Guilherme and Nuno C. G. Horta, Analog Circuits and Systems Optimization Based on Evolutionary Computation Techniques, *Studies in Computational Intelligence*, 2010.

[4] M. Karmani, C. Khedhiri and B. Hamdi, Analog Integrated Circuit Design and Testing Using the Field Programmable Analog Array Technology, *IJAET*, Volume 1, Issue 4, 2011.

[5] P. Chow, S. O. Seo, J. Rose, K. Chung, G. Paez-Monzon, and I. Rahardja, The Design of an SRAM-based Field-programmable Gate Array-part I: Architecture, IEEE Trans. on Very Large Scale Integration (VLSI), 1999.

[6] T. Hall, D. Anderson and P. Hasler, Field-Programmable Analog Arrays: A Floating-gate Approach, 12th Int'l Conf. on Field Programmable Logic and Applications, Montpellier, France, 2002.

[7] P. Dong, Design, Analysis and Reat-time Realization of Artificial Neural Network for Control and Classification, PhD thesis, 2006.

[8] ANADIGM Data Sheet, 2003-2010.

[9] M.White and Yuan Chen, Scaled CMOS Technology Reliability Users Guide, NASA Electronic Parts and Packaging (NEPP) Program, 2008.

[10] M, Bushnell & Agrawal, Vishwani, Essentials of Electronic Testing for Digital, Memory, and Mixed-Signal VLSI Circuits, 2002.

[11] M. Karmani, C. Khedhiri and B. Hamdi, Design and Test Challenges in Nano-scale Analog and Mixed CMOS Technology, *International Journal of VLSI Design & Communication Systems (VLSICS)*, Vol. 2, No. 2, 2011.

[12] Huertas, J.L, Test and Design-for-test of Mixed-signal Integrated Circuits, Springer 2004.

[13] V. Agarwal, Simplify SoC Development with Embedded Testing, Tech. paper, 2002.

[14] J. T. Healy, The New DFT Reality at 90nm, SOC central pub, 2005.