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A Novel Study of the Advantages of STSC Logic Over Other Logic Styles for Ultra Low-Voltage and Low-Energy Digital Application at 45 nm Process Technology

Sajib Roy[1], Md. Murad Kabir Nipun[2] & J. Jacob Wikner[3]

[1]Department of Electrical Engineering, Linköping University, Linköping, SWEDEN

[2]Department of Electrical Engineering, Linköping University, Linköping, SWEDEN

[3]Department of Electrical Engineering, Linköping University, Linköping, SWEDEN

(E-mail: sajro823@student.liu.se[1], murni413@student.liu.se[2], Jacob.Wikner@liu.se[3])

Abstract: The purpose of this paper is to focus on the applicability of sub-threshold source coupled logic for implementing digital circuits and systems that runs at a very low voltage and promise to provide desirable performance with excellent energy savings. Sectors like bio-engineering and smart sensors development require energy consumption to be effectively low for longer battery life. Alongside achieving ultra-low power specification, the system must also be reliable, robust and perform under harsh conditions. In this paper logic gates are designed and analyzed, using STSCL, for implementation of digital sections in small sized smart-dust sensors which should operate at very small supply and consume extremely low power. For understanding the performance of STSCL in fields of ultra low-power and energy; 8-by-8 array multiplier, fifth-order FIR Filter and ninth-order FIR Filter have been designed at schematic level. Circuits and systems have been simulated for different supply voltage, scaling as minimum as 0.2 V, at different temperature values (-20°C and 70°C) and at a process technology of 45 nm. Architectures assigned for the FIR filters and array multiplier have been conventional and taken from CMOS logic based designs. The simulated results are studied, analyzed and compared with other sub-threshold logic styles including sub-threshold CMOS and Null-Convention Logic (NCL). The results indicate upon the advantage of STSCL based digital system over other logic styles, by providing results of energy consumption of 0.15 pJ for ninth-order FIR filter, at -20°C.

Keywords: STSCL, PDP, PMOS Load Device, Sub-threshold Amplifier, FIR Filter, Serial-Parallel Multiplier.

1. INTRODUCTION

The concepts of utilizing ultra-low power specification solely depend on the application and the purpose for which ultra-low energy usage will be served. This paper addresses the use of sub-threshold circuits for Smart sensors. The most important requirement for deploying such sensors are them designed in smaller size and running them at very low supply voltage. This is mandatory when we are considering running the sensors by exploiting energy harvesting techniques from surrounding environment where the sensors will be employed. The energy harvesting techniques are more noteworthy for Smart sensors as these techniques eliminate the use of having expensive and long lasting batteries. Utilizing the energy harvester economically and consistently managing the performance of the driving system at very low supply, urges the requirement of designing digital system that uses sub-threshold circuitry techniques. Smart sensors mainly inquire operation under harsh level and conditions with the power availability being scarce. Sub-threshold operation mitigates the issue of minimizing power usage, but this do come with some drawbacks which include the degradation in the system throughput, variation of the system stability and functionality with process and temperature variation and most importantly design area usage. Thus need for a different sub-threshold logic style instead of operating CMOS at sub-threshold regime is highly appreciable in the fields of ultra-low power applications. This is mainly due to the difficulty and additional cost of maintaining CMOS under sub-threshold region of operation. The additional cost originates as conventional digital systems and architectures will not perform at sub-threshold region and hence modification at both device and system level will be necessary for maintaining CMOS based design to perform desirably at sub-threshold region of operation. But although sub-threshold logic requires a large design area, considering operating frequency of the sub-blocks within the system under Kilohertz range and extreme low power being the target, some sacrifice in terms of design area can be tolerated. One key point has to be mentioned regarding the focus of this paper, which is not to design the whole sensor mode, but instead to find and propose the applicability of using a different kind of logic style

(operating at sub-threshold region) to implement the sensor modes that can run at harsh and extreme conditions for a very low supply voltage, while maintaining low energy consumption with desirable performance level. In section 2 of this paper we look at the basic STSCL gates that will be essential to create the STSCL based standard cell library and later on design the fifth and ninth-order FIR filters. Alongside this focus is given on achieving the minimal configuration at which the gates can operate. Section 3 and 4 emphasizes on the implemented architecture of an 8-by-8 Multiplier, the fifth and ninth-order filter in STSCL gates, and comparison of their performance with CMOS and other sub-threshold gates. The comparisons have been made based on the differences in Power-Delay Product (PDP) value. Also these section discuses the possible strategies on improving the performance of STSCL based system.

2. SUB-THRESHOLD SOURCE COUPLED LOGIC GATES

STSCL gates are differential source coupled logic gates that operate in the sub-threshold region. In Figure 1, an STSCL inverter gate (also a buffer because of the differential characteristics of STSCL) is shown with a PMOS load whose body terminal is connected to its drain. This results in a reverse-biased diode within the PMOS transistor that creates a high-resistive loading device. This is needed to maintain a desirable output swing [3] for the STSCL inverter.

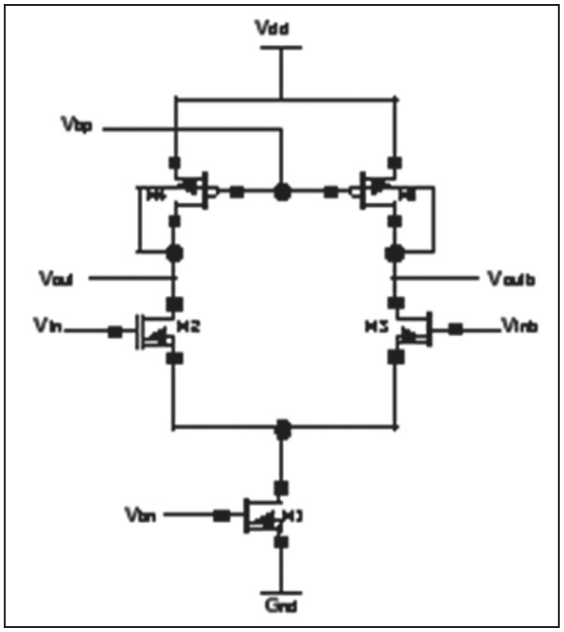

Figure 1: Schematic of a Differential STSCL Inverter/buffer

In addition, each logic gate requires a bias circuit, shown in Figure 2, which sets the voltages on the tail NMOS current source and the PMOS loads. The tail bias current controls the current through the STSCL gate, i.e., it also fixes the power consumption to a constant value. The range of this bias current, for each gate, can vary from a range of 250 pA to 10 nA. The non-ideal current source used for this fixed amount current flow is shown in Figure 3. The range of the current flow is varied by changing the aspect ratio (W/L) of the three stage current mirrors, as shown in the schematic. This range and value of the bias current will depend on the speed of the gates at which they will be operated. A bias current of 250 pA is the minimum limit that has to be provided for the desirable operation of a STSCL circuit. The maximum operating frequency that can be achieved at this bias can be calculated using the slew rate condition,

$$SR > 2 \,.\, pi.\, f_{max} \,.\, V_{swing} \tag{1}$$

The slew rate can be evaluated from I_{bias}/C_{gs} where,

$$C_{gs} = E \,.\, A/2 \,.\, t_{ox} \tag{2}$$

In our process this equals approximately 200 kHz.

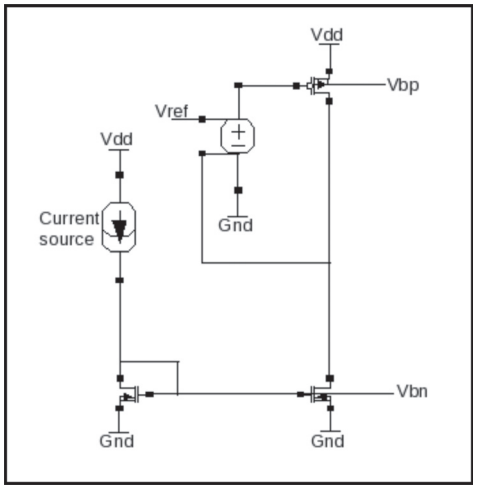

Figure 2: Schematic of the Bias Circuit for STSCL

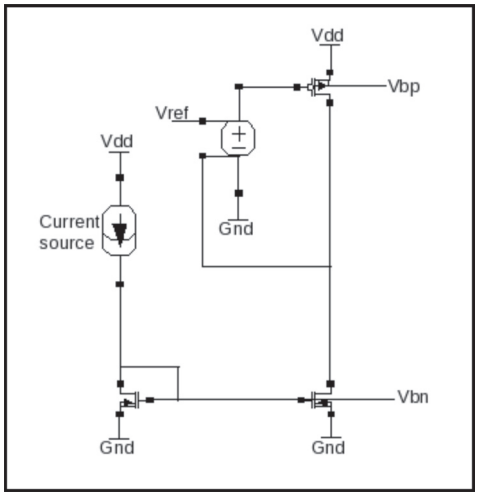

Figure 3: Schematic of the Non-ideal Current Source for STSCL

All the MOSFET devices in the STSCL gate have a low threshold except for the tail NMOS and its corresponding biasing components. The latter devices use high thresholds to minimize the leakage through the bias circuit itself. The only initial complexity that might arise designing a system using STSCL is the overall wiring, due to dual rail input/output configuration.

The motivation and reason behind using a differential logic style in the filter is not only to achieve high noise immunity. In this case the differential logic form allows the system to be able to run at really low voltage and utilize the sub-threshold regions. Further on, the effects due to sub-threshold leakage current is also reduced. The only leakage contributors in STSCL circuits are gate [4] and junction leakage. A notable thing to remember is that at 45 nm the gate leakage is comparatively more dominant than junction leakage [5]. The operating speed for STSCL gates are also a part of concern as the speed of operation directly impacts the energy consumption and performance due to the bias current through the gate, hence the power consumption. Thereby a tradeoff has to be made at the initial phase, based on the design requirement.

2.1. STSCL Bias Circuit

The bias circuit (Figure 2) has to be well designed and has to be insensitive to PVT variations and should consume a very leakage current, since otherwise the overall power consumption increases. The aspect size ratio (W/L) for the mirror circuit has been kept constant and the NMOS devices use high threshold values to reduce leakage. The gain of the amplifier shown in Figure 2 has been kept to a low value approximately 0.01. Any gain value above the value of 1 causes the STSCL gates to not work or function at sub-threshold region. The temperature conditions include operation at and -20°C and 70°C.

2.2. Sub-threshold Folded-Cascode Amplifier

The differential amplifier mentioned in sub-section A., folded-cascode architecture has been used. Figure 4 shows a schematic view of the amplifier with modified PMOS load device. Similar PMOS load devices have been used for the design of the amplifier's architecture in order to operate it at sub-threshold region. Even-though this architecture uses more number of transistors but it is easily applicable to operate at very low voltage. Others architectures like two-stage OTA can also be which would require less number of transistors.

2.3. XOR, OR, AND, and DFF in STSCL

Exclusive or (XOR/XNOR), or (OR/NOR), and (AND/NAND) gates, along with flip-flops (DFF/DNFF), and Full-Adder are typically the most commonly required gates such that a digital filter and multiplier applicable to smart

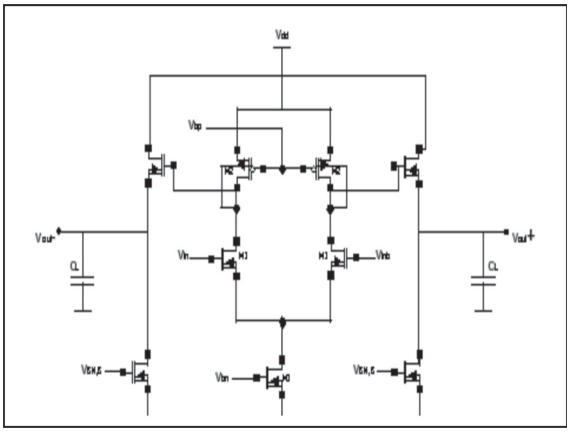

Figure 4: Schematic of the Sub-threshold Folded-cascode Amplifier

sensors can be implemented. The differential dual rail gates are all designed to operate in sub-threshold region at supply voltages down to 0.2 V. The allowed bias currents per stage equal to minimum value of 250 pA. The widths of the PMOS load devices are 135 nm and the NMOS input devices have to have stronger driving capability and the widths are chosen to be 675 nm. A further higher value of NMOS width can be chosen but with sacrificing the output swing. An allowed value of 40 mV has been kept as the maximum output swing deviation for each gate. The width of the PMOS has to be low to achieving a high load resistive value, which is highly required for running the gates at sub-threshold region. The circuit schematics for the XOR, and OR gate are given in Figure 5, AND gate and D-Latch are given in Figure 6. The simulations for XOR, OR, AND gates are performed with inputs at a rate of 10 kHz. For the DFF a clock frequency of 44.1 kHz is applied as the clock signal with the input data rate, fixed as before, at 10 kHz and an output toggling probability of 50 %. The DFF has been designed using two D-Latches implemented in master-slave configuration. The simulated results of each gate at different temperatures and a 0.2-V supply and 250 pA bias currents are given in Table 1.

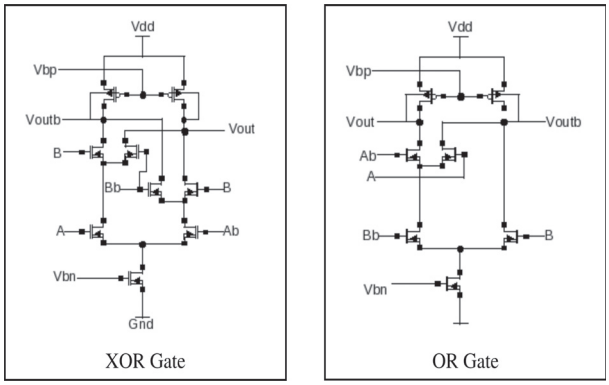

Figure 5: Schematic Diagram of STSCL Gates (XOR Gate, OR Gate)

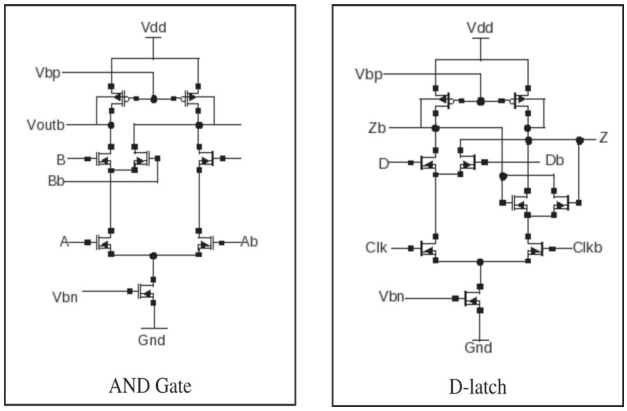

Figure 6: Schematic Diagram of STSCL Gates (AND Gate, D-latch)

Table 1
Performance Simulation Results of STSCL Gates

Logic	*Temperature [°C]*	*Power [nW]*	*Delay [μs]*
XOR/XNOR	-20	0.152	2.52
	70	1.11	0.096
OR/NOR	-20	0.157	1.489
	70	1.15	0.129
AND/NAND	-20	0.15	1.422
	70	1.15	0.135
Logic	*Temperature [°C]*	*Power [nW]*	*Delay [μs]*
DFF/DNFF	-20	0.442	2.97
	70	3.366	0.152

3. STSCL BASED DIGITAL ARCHITECTURES

3.1. An 8-by-8 Array Multiplier

Prior to designing the finite impulse response length (FIR) filter using STSCL, an 8-by-8 array multiplier is designed in order to test and verify the significance of using STSCL over normal CMOS based standard logic cell library.

The array multiplier has a conventional tree-based structure and the block diagram is shown in Figure 7. The structure has been designed in STSCL at a 0.2 V supply voltage with a 250 pA bias current per stage. In CMOS we had to use a supply voltage of 0.5 V to guarantee operation using the standard cells at hand. The circuit operated at -20°C. The simulated power delay product (PDP) turned out to be comparatively smaller for STSCL than CMOS.

One important concern to come up from the simulation result is the additional chip area which the STSCL based design will occupy compared to conventional CMOS. An estimated area has been obtained from the layout of the 8-by-8 multiplier designed in two different logic styles (STSCL and standard-cell CMOS) and the results are shown in Table 2. The tabulated results show that the area for STSCL is three times larger comparing to CMOS as the total design area includes more than one bias circuit for the design of the whole multiplier. This was partly done to achieve desirable performance from the multiplier, which was not achievable from using single bias circuit. Also the delay for the STSCL is more than 35% longer compared to CMOS but the power delay product is lower. The results show that the overall energy consumption for an 8-by-8 multiplier is less using STSCL than CMOS.

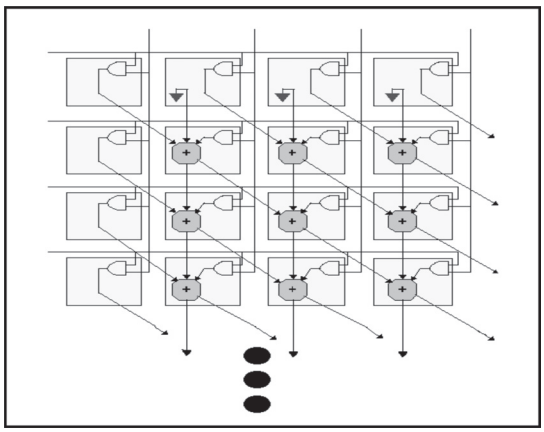

Figure 7: Architecture of an 8-by-8 Array Multiplier

Table 2
Performance Comparison for 8-by-8 Multiplier

Logic	*STSCL*	*CMOS*
PDP [fJ]	302.4	313.15
Delay [μs]	52.47	38.65
Area [μm^2]	330	110

3.2. STSCL Based Digital Filter

The transposed direct form architecture (shown in Figure 8) is chosen for the fifth and ninth order FIR filter since it is a conventional, widely-used and foremost verified structure. The filter has a serial-input and serial-output form with a sampling frequency of 44.1 kHz. For the multiplication with fixed coefficients a five-bit serial/parallel multiplier [6] has been used with the coefficients being represented in two's complement form. No optimization with respect to coefficients has been performed as the comparison between the performance of the STSCL and CMOS have been the prime focus of this work.

The supply voltage using STSCL is 0.2 V with a bias current at 250 pA per stage. For STSCL 0.2 V is the limit up to which the supply can be reduced and system can be operated. The basic tryout for the different supplies allowed seeing how well a system could perform under critical situation while STSCL gates have been configured to run at their minimum operating specification. Simulations have been run using Cadence Virtuoso v6, for STSCL logic

at -20°C temperature and the power-delay product is calculated from product of power consumption with the overall system sampling period. The results of the PDP along with the delay for the fifth-order filter are shown in Table 4. The Table 3 reflects on the comparison of the STSCL based multiplier and ninth-order FIR filter with other sub-threshold logic styles.

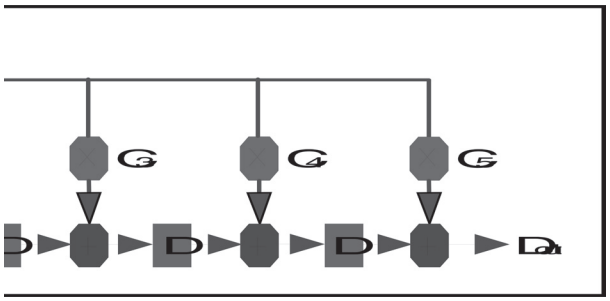

Figure 8: Block Diagram of a Fifth-order FIR Filter Using Transposed Direct form Architecture

Table 3
Power Delay Product and Supply Voltage Comparison of STSCL Based Circuits with Other Sub-threshold Logic Styles

Article	*Circuit*	*Process [nm]*	*Applied Logic*	*Temper-ature [°C]*	*Supply voltage [mV]*	*PDP*
[7]	Ninth order FIR Filter	65	sub-CMOS	25	0.22	1.33 pJ
[8]	Fifth order FIR Filter	65	NCL	25	0.3	4.56 pJ
[9]	8-by-8 multiplier	350	VT-sub-CMOS	25	0.5	0.672 pJ
[3]	8-by-8 multiplier	180	STSCL	25	0.35	1 pJ
This paper	8-by-8 multiplier	45	STSCL	-20	0.2	0.3 pJ
This paper	Ninth order FIR filter	45	STSCL	-20	0.2	0.15 pJ

Table 4
Power Delay Product Comparison of the STSCL Based Fifth-order Filter at Different Operating Temperatures

	Logic	*STSCL*
Temperature [°C]	-20	70
Logic	STSCL	
PDP [fJ]	600.4	45.81
Delay [µs]	9.47	1.06

4. CONCLUSION AND FUTURE WORK

The simulation results in Table 3 and Table 4 depict the performance for STSCL at both extreme and normal extreme condition to be comparatively better than other sub-threshold logic styles including CMOS and NCL. The results have been shown for schematic level at 45 nm process at a supply voltage of 0.2 V. The most important factor found in the simulations is the energy consumption for STSCL being less than other sub-threshold logic styles which suggests trying out further implementation of all the digital components for applications, like smart sensors, in STSCL.

The simulation results shown in this paper are currently based on the schematic level designs, but proper understanding of STSCL and its benefactors will require implementation of the following designs on chip level. This will enable to evaluate the STSCL logic based designs more accurately.

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