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10.56 GHz TRANSIMPEDANCE AMPLIFIER (TIA) USING DYNAMIC BODY BIAS TECHNIQUE WITH LOW POWER DISSIPATION OF 0.438mW

Priya Singh[1], Vandana Niranjan[2] , Ashwni Kumar[3]
[1,2,3]Department of Electronics and Communication Engineering
Indira Gandhi Delhi Technical University For Women Kashmiri Gate, Delhi, India

Abstract: In this paper a low power , low voltage transimpedance amplifier (TIA) is designed using dynamic body bias technique utilizing regulated gate cascode (RGC) configuration thus can be called as D-RGC. The circuit operates at supply voltage of 1V with power dissipation of 0.438mW only this is the main advantage. Simulation is carried out using 180nm gpdk technology node. For bandwidth enhancement shunt peaking method is also employed further. The dynamic body bias technique is used in common source configuration to provide feedback to main amplifier thus threshold voltage changes according to input signal leading to less leakage current. The proposed TIA provide the low power consumption due to less leakage current and high transconductance due to body effect. Thus use of dynamic body biasing in TIA improves the input impedance as compared to conventional TIA thus bandwidth of transimpedance amplifier is increased by nearly 10 times.The transimpedance gain is increased by 7.79 %.

Keywords: TIA, RGC, Cascode, Dynamic Body Bias, -3dB bandwidth.

1. INTRODUCTION

Transimpedance amplifier (TIA) is basic building block of analog systems in which obtained input signal is current signal and output is amplified voltage signal . For example in optical communication, bio medical devices and so on. The main characteristics of TIA are low input impedance due to current as input signal and low output impedance due to voltage as output signal. The gain is measured in ohms and known as transimpedance gain i.e. ratio of output voltage and input current. All applications of TIA require higher bandwidth to achieve high data rate and higher sensitivity to work on even small amplitude current. Based on the literature study various types of transimpedance amplifier are designed but broadly it can be classified as 4 types- common gate TIA, common source TIA , Regulated Gate cascode (RGC) TIA and differential TIA . RGC TIA is mainly preferred since RGC TIA offers isolation to parasitic capacitance at input node so that input impedance is low as compared to other topologies. Till now all the TIA have been implemented using CMOS, but in this era of nanotechnology CMOS is facing some drawback while implementation for VLSI circuits. Major challenges are decreased threshold voltage, increased leakage current, device heating, high power dissipation and so on. Based on the challenges faced various RGC TIA has been designed to improve the characteristics according to requirement resulting in complex circuit and increased die area. This paper presents a design method of TIA to improve the overall performance without much tradeoffs between characteristics. Dynamic body bias technique is used instead of normal MOS to increase the overall transconductance of the circuit which improves the input impedance. Section 3 in this paper explains the conventional RGC circuit and its drawback. Further section 3 includesthe advantage of using dynamic body bias technique instead of normal MOS and its small signal model , proposed TIA with its circuit description and small signal analysis and section 4 presents the simulation results obtained and comparison with previous TIA.[1-16]

2. CONVENTIONAL TIA

As depicted in figure 1 conventional TIA circuit have common gate MOS and common source MOS as feedback. General equation of input impedance and gain of the circuit is as follows[11]:

$$\text{Input impedance} = \frac{1}{g_{m1}(1+g_{m2}R_2)} \qquad (1)$$

$Gain=-\{g_{m1}(1+g_{m2}R_2)\}R_1$ (2)

Here g_m represents transconductance of both the MOS.

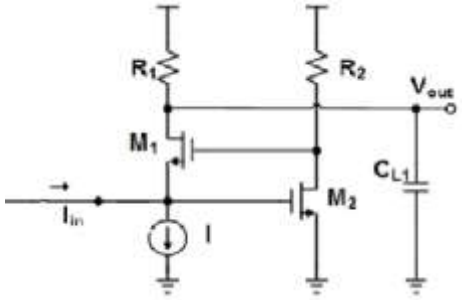

Fig1 conventional TIA circuit [11]

In this circuit common source MOSFET reduces the effect of parasitic capacitance on bandwidth of the circuit but its drawback is there is a severe need of tradeoff between gain, bandwidth and noise. Various work was done for improvement of conventional RGC [11-16] . But despite of all mechanism included which makes the circuit more complex lots of circuit parameters suffered such as power dissipation, bandwidth, voltage swing range and so on.

3. PROPOSED CIRCUIT

In this paper we had proposed the RGC using dynamic body bias technique thus can be called as D-RGC TIA. But first we need to know why dynamic body bias technique can replace CMOS in this RGC architecture as explained in section 3.1.

3.1 Dynamic Body Bias Technique

CMOS device are not efficient to use in low power , low voltage application due to leakage currents , reduced gate overdrive and small area of CMOS. Dynamic body bias technique in which gate and body terminal are tied together is a solution to this problem without even changing the structure. Thus dynamic body bias technique is compatible with all existing CMOS circuits as well. In normal MOS an important condition for saturation region is Vgs> Vth , but in dynamic body bias technique small signal at input terminal can generate saturation voltage at output terminal. The working principle of dynamic body bias technique is as follows : For NMOS Vbs is greater than zero and for PMOS Vbs is smaller than zero thus threshold voltage also vary accordingly. Input is given through both gate and body terminal since both are shorted thus Vbs = Vgs. Due to voltage at body terminal potential in channel region is controlled by both gate and body. This leads to addition of transconductance due to body terminal i.e gmb . [8-10]This circuit technique provides an important solution to the threshold voltage scaling limitation thus modulates the threshold voltage of a MOS transistor electronically using body effect, without any technology modification. [17-19].

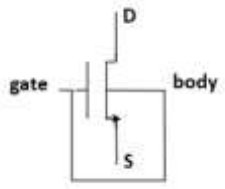

Fig.2 n channel DTMOS

Due to this body transconductance total transconductance increases as shown in equation 3 thus current transport becomes faster compared to normal MOS

$$g_{meq} = g_m + g_{mb.} \qquad (3a)$$

$$\frac{g_{mb}}{g_m} = \eta \approx (0.2 - 0.4) \qquad (3b)$$

Here g_{meq} represents equivalent transconductance of MOS with dynamic body bias, g_m is transconductance of MOS without body bias and g_{mb} is the transconductance in MOS due to body bias. η is specific parameter and its value depends on bias conditions and on the technology used. The effective transconductance of gate and body driven MOS transistor is defined a $g_{meq} = g_m(1 + \eta)$. [18]

As we know the relation between input signal and threshold voltage is described by equation 4 and 5.

$$V_{T0} = 2\Phi_B + V_{FB} + \frac{\sqrt{2q \in sNa\,(2\Phi_B)}}{C_{ox}} \qquad (4)$$

$$V_T = V_{T0} + \lambda(\sqrt{2\Phi_B - V_{BS}}) \quad (5a)$$

$$V_T = V_{T0} + \gamma(\sqrt{\psi s + V_{SB}} - \sqrt{\psi s}) \qquad (5b)$$

Here V_T is the threshold voltage due to body effectΦ_B is the inversion layer potential V_{FB} is the flat band voltage Na is the channel doping , $\in_S$ is the Si permittivity , λ is the channel length modulation coefficient and q is the charge. γ is typically equals to 0.4 $V^{0.5}$ and depends on the gate oxide capacitance, ψs is surface potential in strong inversion and typically is 0.6 V. ψs in equation (5b) is assumed to $|2\Phi_F|$, where Φ_F is Fermi potential

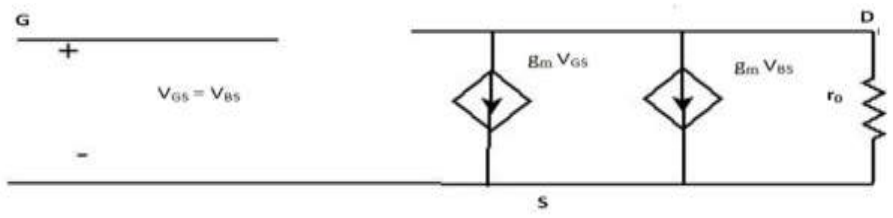

Fig.3 Small signal model of DTMOS [8-10]

From equation 5a as V_{BS} increases V_T decreases and vice versa, thus leakage current probability is very low , so power dissipation is low.DTMOS can work in nanotechnology efficiently due to it dynamic threshold adjustment according to input signal. [17] .It also helps in low power consumption and work on low supply voltage . Figure 3 depicts the small signal model of MOS with dynamic body bias and figure 2 shows symbol of DTMOS. In this model we had assumed the capacitors to be short circuit for small signal.

3.2 TIA USING Dynamic Body Bias Technique

3.2.1 Circuit Description

The circuit as shown in figure 4consist of common gate MOS using dynamic body bias technique M1 with resisistive load R1 ,a resistor Rs to set the bias current through MOS in common gate configuration with dynamic body bias technique. A common source MOS M2 is used as a feedback with resistor R2 . In this circuit inductor L0 act as a shunt peaking device to increase the bandwidth by reducing the charging time of load capacitor C1 at output node. This inductor is optional and added just to see the bandwidth enhancement due to shunt peaking. Here common gate MOS act as main amplifier and M2 and R2 helps in reducing the input impedance by the amount of its

voltage gain. Thus the effect of parasitic capacitance at input node is lowered due to this and bandwidth can increase. Here due to use of dynamic body bias technique instead of normal MOS overall transconductance increases thus current transport also become fast. This helps in further increase of bandwidth. Since threshold voltage of dynamic body bias technique dynamically vary according to input signal probability of leakage current reduces, thus leakage power consumption also reduces. [7-10]

3.2.2 Small signal analysis

Figure 5 depicts the small signal model of the proposed circuit. By assuming at small signal analysis capacitors act as open circuit and inductors as short circuit further equations are derived.

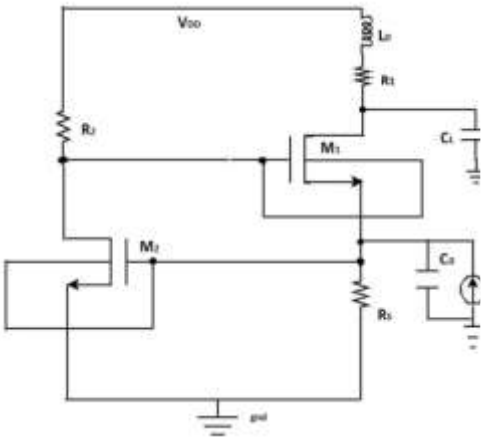

Fig. 4 Proposed D_RGC TIA with shunt peaking

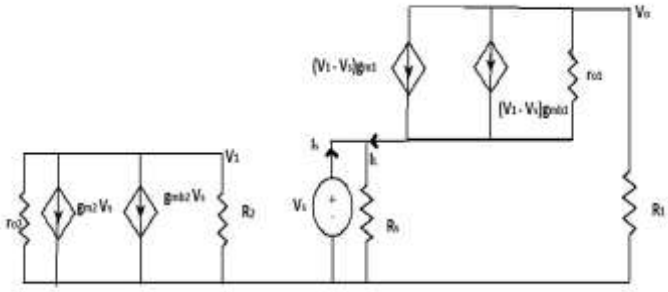

Fig. 5 Small signal model of proposed D_RGC TIA

Here Vs = Vin

(a) Input impedance
At node 1 applying KCL we get

$$V_1 = -g_{meq2}\, V_s\, (r_{o2} \parallel R_2) \qquad (6)$$

At node 2 applying KCL we get

$$g_{meq1}\,(V_1 - V_S) + \frac{Vo - Vs}{ro\,1} + I_S = \frac{V_S}{R_S} \qquad (7)$$

by solving equation 4 and 5 we get input impedance Zin.

$$Zin = \frac{1}{g_{meq\ 1}\,(1 + g_{meq\ 2} R_2)} \qquad (8)$$

Here $g_{meqi} = [g_{mi} + g_{mbi}]_{i=1,2}$

From equation 6 it is clear that due to increased transconductance of MOS as compared to normal MOS input impedance of dynamic body bias technique using RGC is reduced further thus better isolation from parasitic capacitances.

(b) Voltage gain

Since gain = Vo/ Vs

As shown in small signal model

$$Vo = -I_L R_1 \qquad (9)$$

By applying KCL

$$I_L = Vs/ Rs - I_S \qquad (10)$$

By equation 9 and 10 further derivation we had obtained

$$Gain = - \{g_{meq1} (1+ g_{meq2} R_2) + 1/ R_S \} R_1 \qquad (11)$$

For increased -3 dB bandwidth gain of the amplifier should be high. From equation 11 it can be seen that dynamic body bias technique offers higher gain as compared to normal MOS due to high transconductance. Thus greater bandwidth can be obtained. For noise analysis considering the extra current source due to body effect an extra noise source is also added . Thus noise due to use of dynamic body bias technique circuit may increase. The amount of increased noise is shown in simulation and results section.

4. SIMULATION AND RESULTS

Simulation is carried out using cadence virtuoso software . Technology node of 180nm with gpdk file is used for implementing both conventional and proposed circuit **.**

4.1 Circuit parameter analysis

The AC analysis is performed the conventional and proposed RGC circuit to obtain the -3dB bandwidth. As shown in figure 6 -3dB bandwidth of proposed circuit is increased due to use of dynamic body bias technique. As quoted in [6,7] decrease in input impedance lead to increase in bandwidth for RGC. From equation 8 it is clear that input impedance for proposed circuit is low as compared to conventional RGC. Thus effect of parasitic capacitance at input node is lowered which leads to increase in bandwidth.Similarly as shown in equation 11 the gain of D-RGC TIA is high and this is verified by AC analysis . Gain is increased by 67.5% in proposed RGC.

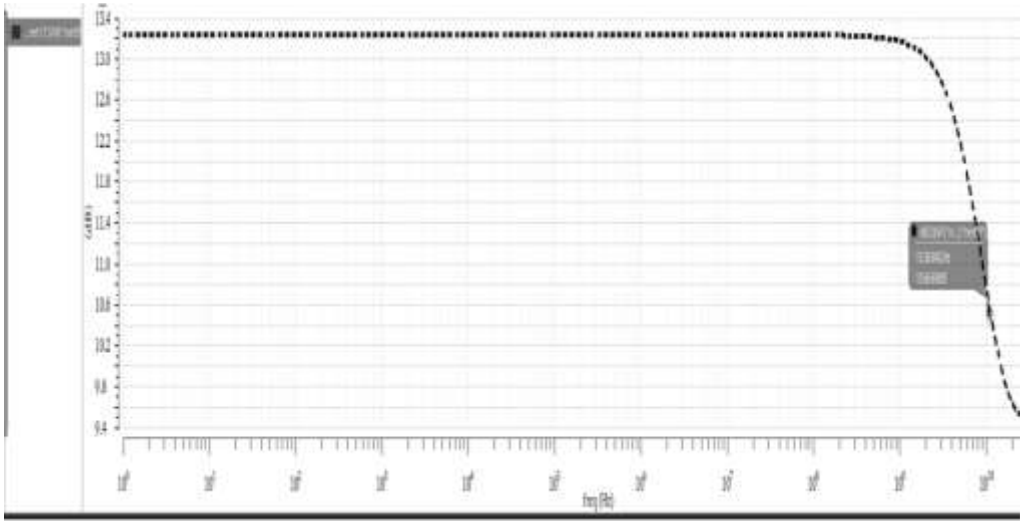

Fig. 6AC analysis – Gain plot of DTMOS RGC TIA

We had performed the Sparameter analysis to obtain the input and output impedance of conventional and proposed RGC. The input impedance is reduced by 63.81% and output impedance is reduced by 2.36 % only. The results are compared in table 3 The transimpedance gain is increased by 7.79% by proposed RGC. For its calculation transient analysis is performed to know the output voltage and input current ratio as shown in figure 7.

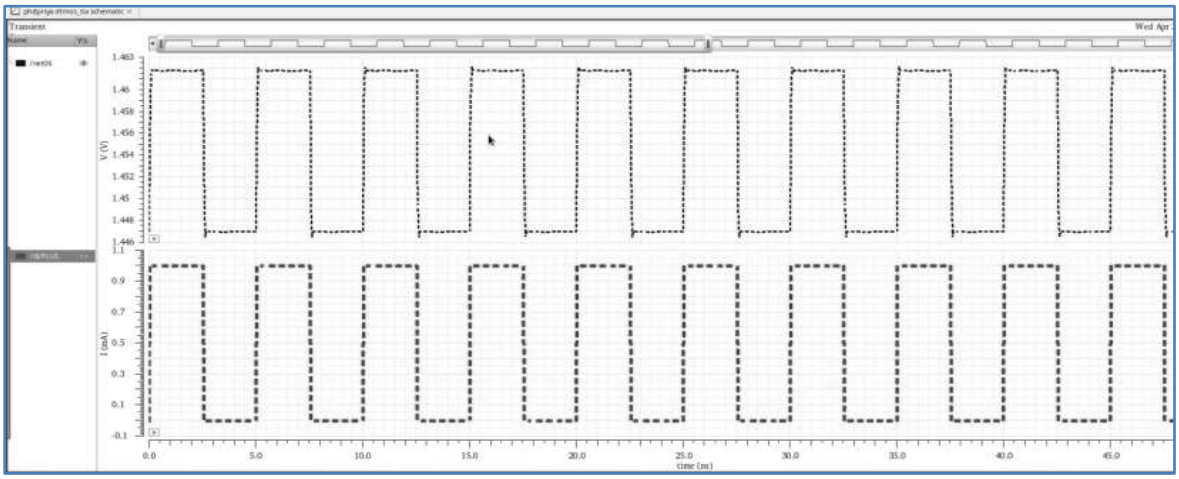

Fig. 7 transient analysis of D_RGC TIA

4.2 Parametric analysis and noise analysis

For the noise analysis since input is current and output is voltage thus we had taken input noise in current form and output noise in voltage form to know the exact effect on input signal and output signal.The proposed circuit introduces one more noise source due to body terminal in action . Thus we had obtained increased input noise . But the noise generated is very small as compared to input signal thus it is not the major drawback for application of this TIA. Further improvement can be done using various noise reduction techniques. Whereas output noise is reduced by 51.32% for DTMOS TIA thus , it will contribute less noise towards other blocks of system in which it will be used.The noise analysis is compared in table 3. We had employed the shunt peaking method in normal RGC structure to know its effect on badwidth enhancement plot shown in figure 8 is analysed and this shunt peaking inductor helps in increasing the bandwidth by 33.52% as compared to normal D-RGC . In Fig.9 bandwidth of D-RGC TIA with shunt peaking technique is analysed using monte carlo analysis. The montecarlo analysis for bandwidth of proposed DTMOS RGC TIA to know the process variation and matchinng effect on the circuit here obtained maximum bandwidth is 13.5 GHz and mean badwidth is 13.4 GHz with deviation of 334.7MHz. It can be concluded with this analysis that considering all process corners and process analysis of matching effect the obtained bandwidth is very much higher then conventional RGC TIA. We had performed parametric analysis of proposed circuit at different temperature and load capacitors to know its behaviour at the extreme conditions. The result obtained in fig 10 is arranged in table 1. From table 1 we can see that at extreme negative temperature gain is decreased very less but at extreme positive temperature it is increased. Change in load capacitor is not varying the output voltage.

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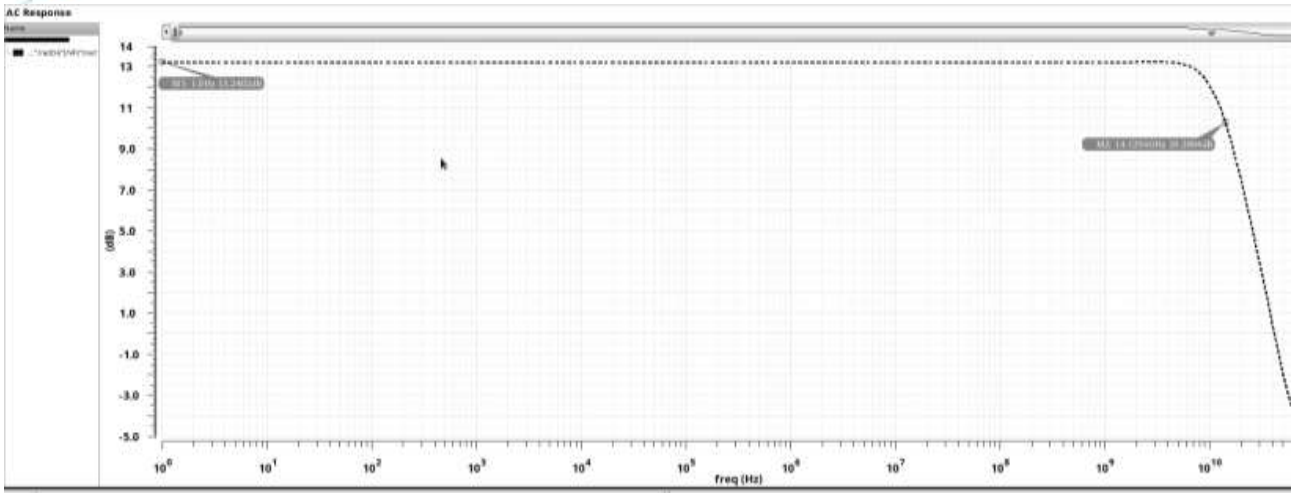

Fig.8 AC analysis – Gain plot of DTMOS RGC TIA with inductor

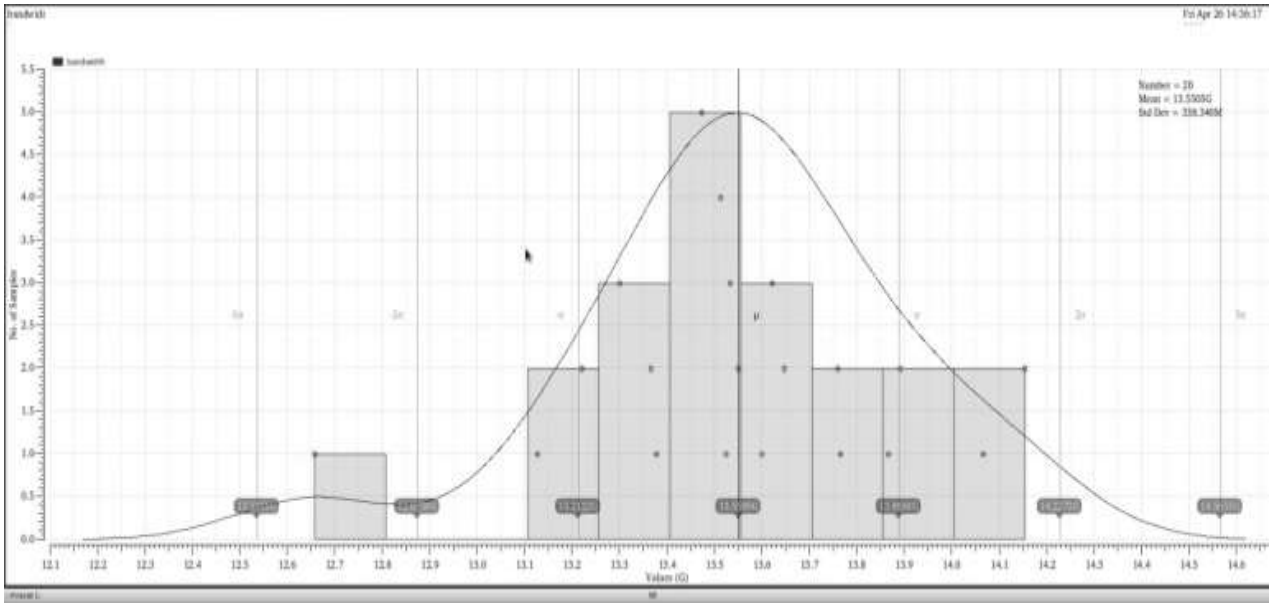

Fig.9. Monte Carlo analysis of bandwidth of D_RGC TIA with shunt peaking techniquue

Table 1: Parametric analysis of gain plot at different Temperature and load capacitors

S.No.	Load Capacitor (fF)	Temperature (C)	Output (mV)
1	50	-40	895.6
2	175	-40	895.6
3	300	-40	895.6
4	50	50	939.1
5	175	50	939.1
6	300	50	939.1
7	50	140	958.0

8	175	140	958.0
9	300	140	958.0

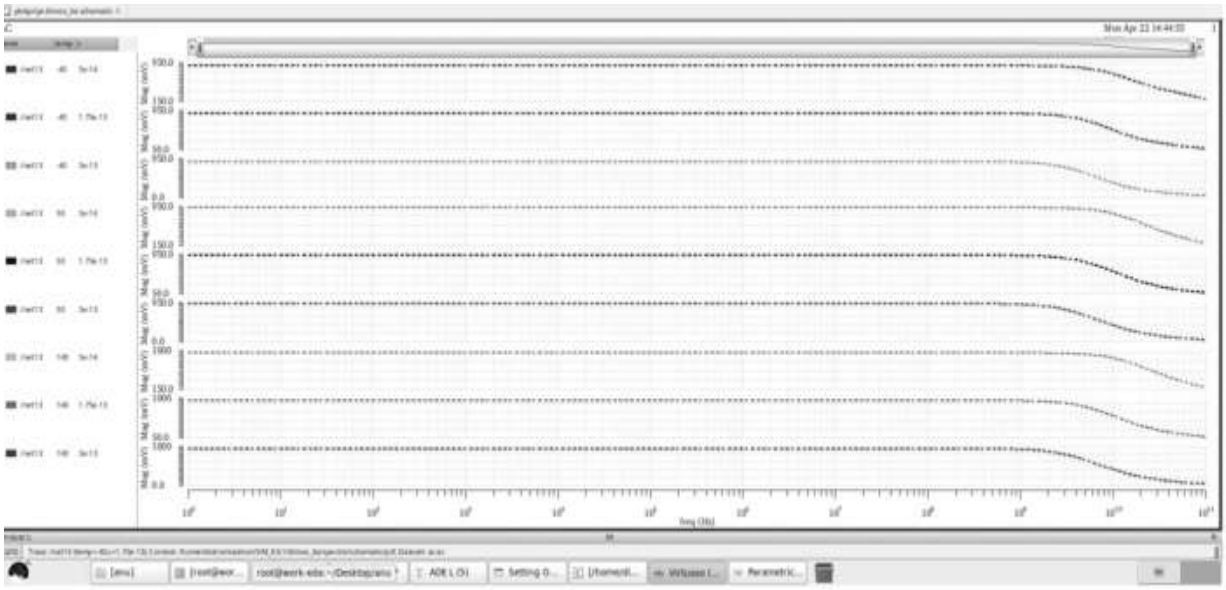

Fig.10 Parametric analysis of Gain plot Of D_RGC TIA at different temperature and load capacitors (a)merged plot (b) separated plot

4.5 COMPARATIVE ANALYSIS

Mathematical analysis had shown that input impedance and gain of D_RGC TIA is improved as compared to RGC TIA. In these equations $g_{meqi} = [g_{mi} + g_{mbi}\ ]_{\ i=\ 1,2}$. Thus this helps in improving the bandwidth further. Comparison of RGC TIA and D_RGC TIA is done in table 2 and 3. From this comparative table we can see that analysis has shown that bandwidth of D_RGC TIA is increased by10 times nearly, gain and transimpedance gain is increased by 67.5% and 7.79 % respectively. Further input impedance and output impedance is also improved by 63.81% and 2.36% respectively. Input noise in terms of current is increased by 2.04 times but output noise is reduced by 51.32 % so further work can be done for noise improvement. Main characteristics which had improved drastically is power consumption i.e by 99.48%. This makes D-RGC TIA very efficient to be used in application where power consumption is important feature to be controlled. Shunt peaking had increased the bandwidth of proposed D_RGC TIA by 33.52 %. as compared in table 4.

Various other research had done on RGC [10-16]. A comparitive study of some of the latest RGC is done in table 5. It can be seen from the literature studied that only by replacing a CMOS with dynamic body bias technique MOS we can work on very low voltage and obtain high bandwidth and gain without inco-orperating any complex circuitry. Use of Dynamic body bias technque in TIA circuit had also reduced power dissipation to lowest value as in authors knowledge.

Table 2 : comparison of equations of conventions and proposed RGC

Characteristics	RGC TIA (conventional)	D_RGC TIA (proposed)
Input impedance equation	$\frac{1}{g_{m1}(1+g_{m2}R_2)}$	$\frac{1}{g_{meq1}(1+g_{meq2}R_2)}$
Gain equation	$-\{g_{m1}(1+g_{m2}R_2)\}R_1$	$-\{g_{meq1}(1+g_{meq2}R_2)+1/R_S\}R_1$

Table 3 : Comparitive study of RGC and D_RGC TIA

Circuit parameters	Supply voltage(V)	Band-width (GHz)	Transimped-ance gain (dBohms)	Gain (dB)	Input imped-ance (mohms)	Output impedan-ce (mohms)	Input noise (nA/sqrtHz)	Output noise (uV/sqrt/Hz)	Power consum-ption (mW)
RGC TIA	1.8	1.12	59	8	912	973	43.65	3.384	85
D_RGC TIA	1	10.56	63.60	13.4	330	950	89.27.	1.647	0.438

Table 4 : Shunt peaking effect on D_RGC TIA

Circuit parameters	Supply voltage (V)	Technology node (nm)	Bandwidth (GHz)
D_RGC with shunt peaking	1	180	14.10
D_RGC without shunt peaking	1	180	10.56

Table 5: Comparitive study of different RGC with proposed dynamic body bias technique RGC

Ref. No.	Year	Topology /technique	Power supply (volts)	Gain dB(ohms)	BW (GHz)	Power dissipation mW
[11]	2004	RGC	5	58	0.950 MHz	85
[12]	2006	RGC	2	52	7.6GHz	34
[13]	2007	RGC	1.8	53	8GHz	13.5
[14]	2012	RGC		52	35GHz	-
[15]	2015	RGC	3.3	61	15GHz	32
[16]	2015	RGC	-	-	9GHZ	-
[17]	2015	RGC	1.5	50	7GHz	-
Proposed RGC	2019	D-RGC	1	63.60	10.56 GHz	0.438

5 CONCLUSION

Dynamic body bias technique is implemented using triple well CMOS technology thus latch-up problem is solved. This technique exhibits merits over other body bias techniques in terms of higher transconductance-to-drain current ratio and elimination of additional circuitry for bias voltage generation.It can be concluded from the mathematical analysis and simulation of both conventional and proposed RGC that , proposed TIA is better in terms of power consumption, bandwidth and gain. Only issue encountered is input noise performance is low. Since noise

performance is to be improved various noise reduction techniques can be applied on the circuit . Other than this the proposed circuit is best suited for low voltage , low power and high bandwidth application

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