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Effect of Spacer on the performance characteristics of SiGe HBT

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Abstract: This paper presents an analytical approach to study the effect of spacer layer in SiGe Hetero junction bipolar transistor (HBT) with reference to their DC, AC, and RF characteristics. A theoretical analysis using Gummel-Poon model has been used to validate the data obtained from simulation using ATLAS module of Silvaco software tool. After validation of models, the SiGe HBTs with spacer and without spacer are considered for our observation. The DC, AC and RF characteristics are evaluated and thereafter a comparative analysis has been carried out based on the important characteristics such as I–V behavior, frequency response, breakdown, maximum cutoff frequency, and minimum noise figure for both the cases. It is observed that, with the same physical structure, SiGe HBT with the presence of spacer produced a high current gain (88) compared to a lower value (67) having no spacer layer. In contrast, having spacer layer provides higher cut-off frequency, higher maximum oscillation frequency, and lower minimum noise figure compared to without spacer.
Keywords: HBT; Spacer; SiGe; ATLAS Silvaco Tool.

1. Introduction

SiGe HBT is used for high speed applications due to its excellent RF performance. Silicon based technology is entered into rapidly growing market for wide bandwidth and wireless telecommunications [1]. In Si/SiGe heterojunction bipolar transistor SiGe is used as base material due to high emitter injection efficiency, maximum frequency and lower base resistance [2]. Also SiGe is used in base region to reduce the energy gap E_g to enhance the collector current. HBT is a high speed device in which base is heavily doped than emitter and collector. Therefore base resistance is reduced; as a result the maximum operating frequency is increased. The wider band gap exists between emitter region and heavily doped base region which opposes the flow of hole from base to emitter so that the current gain increases. To get maximum cut off frequency (f_t) and maximum frequency of oscillation (f_{max}) in the SiGe HBT, boron out diffusion has to be restricted during layer growth and high temperature annealing. Out diffusion of boron is occurred from heavily doped base region to emitter and collector which results to create parasitic potential barrier formation at Si/SiGe conduction band interface [3]. The main criterion that needs to be meet for the boron profile in a SiGe HBT is that the boron must be kept within the SiGe layer to achieve full heterojunction action. If the boron penetrates outside the SiGe layer, the metallurgical junction is formed in silicon, rather than SiGe, leading to the formation of parasitic energy barriers i.e this pushes P^+ n base emitter junction into silicon and the junction is formed at Si instead of SiGe region. The metallurgical emitter/base and collector/base junctions are formed in silicon and hence the silicon bandgap is obtained at these junctions. On moving into the SiGe layer, a decrease in bandgap is obtained, which leads to the formation of parasitic energy barriers at both the emitter/base and collector/base junctions. Even very small amounts of boron out-diffusion from the SiGe layer dramatically degrade the collector current and hence the gain. The f_t of the HBT is also degraded, since the potential well formed by the parasitic energy barriers traps charge in the base [4]. This leads to decrease the current gain and maximum operating frequency of the device. So the small width of spacer layer is introduced in both side of heavily doped base region to prevent the formation of parasitic barrier for electron [5]. Spacer is a thin undoped layer which is called an intrinsic layer. No extrinsic carrier has to be doped in this layer. Spacer can be introduced on both side of the base or either one side of the base. Spacer can be of intrinsic layer of SiGe or Si. Spacer layer is introduced into the device for Opposes boron out diffusion, avoid base emitter tunneling, Increases junction breakdown voltage, decrease junction capacitance, improve the stability of the device, remove parasitic barrier for collector current enhancement. A comparative analysis of the HBT with spacer and without spacer has been carried out based on the common figures of merit such as I–V behavior, cutoff frequency, Early voltage, breakdown, and minimum noise figure. The rest of the paper is organized with device structure in section 2, selection of models in section 3, result and discussion in section 4 and finally conclusion in section 5.

2. Device Structure

The vertical layer SiGe HBT is designed using the ATLAS device simulator. The device is a self aligned structure with emitter area A_E= 0.25×1 μm^2 and width W_E=0.2 μm. The width of base is, W_B= 0.07 μm. The collector width is 1.5 μm with doping concentration is 1×10^{17} cm^{-3} and contact is given at bottom layer. The Sub collector layer is 1 μm, n-type doped with doping concentration 2×10^{18} cm^{-3}. The device is doped uniformly with p-type doping at base of 5×10^{18} cm^{-3} and emitter doping with n-type dopant of 2×10^{18} cm^{-3}. Germanium mole fraction of 0.16 is introduced in the base region. The SiGe spacer having 50 A^0 width have considered in the both the side of the base layer. The both the structures are simulated in Silvaco T-CAD simulator and compared between them.

3. Device Modeling

The models which are selected in ATLAS are derived from continuity equation, poissions equation, Maxwell's law and the transport equations. The process of generation, recombination of electrons and holes are related to continuity and transport equation. The simplest model which is applicable to all device technology is drift diffusion model. This model is used here because it links to change transport model which is responsible for carrier recombination and generation. The model is simulated in ATLAS domain in 300k i.e in room temperature. The Fermi Dirac model is used to simulate the heavily doping material in thermal equilibrium conditions. Band gap narrowing model (BGN) is selected due to heavily doping in the base order of 10^{18}cm^{-3} which is most effective in base collector junction. When doping level increase the bandgap separation between valence band and conduction band decreases. Shockley read hall recombination (Srh) model is used to activate the electron and hole life time TAUN and TAUP respectively. During simulation carrier life time is taken 1×10^{-7} for silicon and 1×10^{-8} for silicon germanium. Auger recombination model is introduced for reduction of carrier life time in high carrier densities. The high electric field in base collector junction saturates the free electron. So to model velocity saturation effect on Silicon device parallel electric field dependence (FLDMOB) model is introduced [6].

Analytical Validation

The device structure is designed using ATLAS and the structure is taken from the reference paper [7]. The device is doped uniformly in emitter, base and collector region. The current gain equation of HBT for uniform doping is given as [8]

$$\beta = \frac{D_{nB} W_E N_{DE} N_{CB} N_{VB}}{D_{pE} W_B N_{AB} N_{CE} N_{VE}} e^{\frac{q(E_{GE}-E_{GB})}{kT}} \quad [1]$$

Where β = DC current gain, D_n= Electron diffusion co-efficient in Base (36-112x) cm^2/s ; x is mole fraction of Ge (0.16), D_{pE}= Hole diffusion coefficient in Emitter is 12 cm^2/s, W_E = Width of Emitter is 0.2µm, W_B = Width of Base is 0.07µm, N_{DE} = Donor doping concentration in Emitter is 2×10^{18} cm^{-3}, N_{AB} = Acceptor doping concentration in Base is 5×10^{18} cm^{-3}, N_{CB} = States density in the conduction band of Base is 2.8×10^{19} cm^{-3},N_{CE}= States density in the conduction band of Emitter is 2.8×10^{19} cm^{-3},N_{VB} = States density in the valence band of the base is 0.17 N_{VE}, N_{VE} = States density in the valence band of the Emitter is 1.04×10^{19} cm^{-3}, q = Electronic Charge is 1.6×10^{-19} C, k = Boltzmann's Constant is 1.38×10^{-23} JK^{-1}, E_{GE} = Band gap in Emitter is 1.17 ev, E_{GB} = Band gap in Base is 1.17-0.96x+0.43x^2-0.17x^3, x= Germanium mole fraction which is 0.16 .Ge dependent parameter can be calculated by putting 0.16 in the place of x.. The theoretical value of current gain is 65. From the simulation result current gain is 67. Hence the models are to be considered as validated.

4. Result and Discussion

4.1 DC Characteristics:

The Gummel plots for the HBTs with spacer and without spacer are shown in Figure 1. These plots are indicative of the fact that the SiGe HBT with the spacer has a superior performance in terms of the DC current gain compared to without spacer. The figure is indicative more collector current having same base current when the spacer layer is present. The reason is due to out diffuse of impurities is reduced.

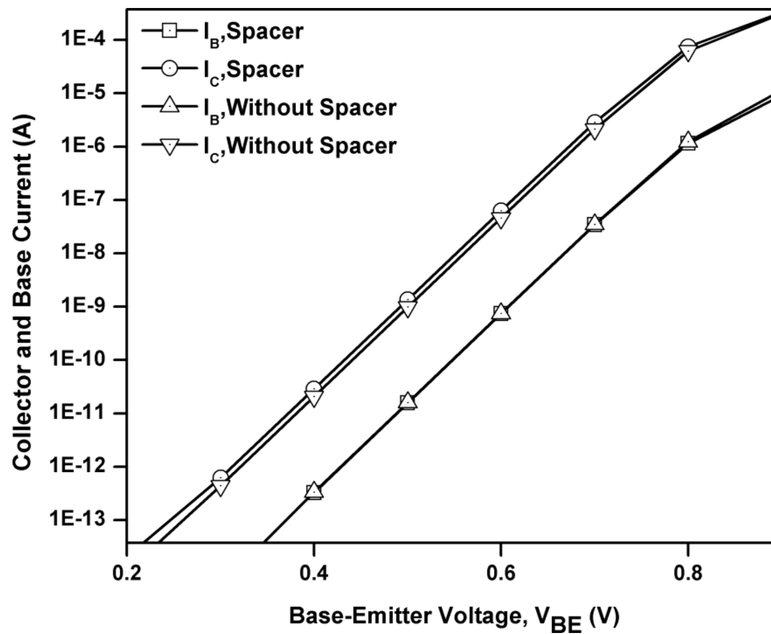

Figure 1: Gummel Plot of the proposed devices

The dc current gain (β) is plotted in Figure 2. The figure indicates maximum β of 88 and 67 respectively for the HBT with spacer and without spacer as against their theoretically calculated values of 90 and 65 determined using Gummel-Poon model described in section 3. The close agreements of the two values in each case justify the use of our simulation model. The high value of DC gain (β=88) in the presence of spacer is a clear advantage compared to the other. The high β in the HBT with spacer can be explained as follows. In the presence of spacer , the dopant which is present in the base start diffuse towards the emitter and collector region. The spacer which treat as here an intrinsic layer opposes the flow impurities to the both direction. Hence more gain is observed compared to without spacer.

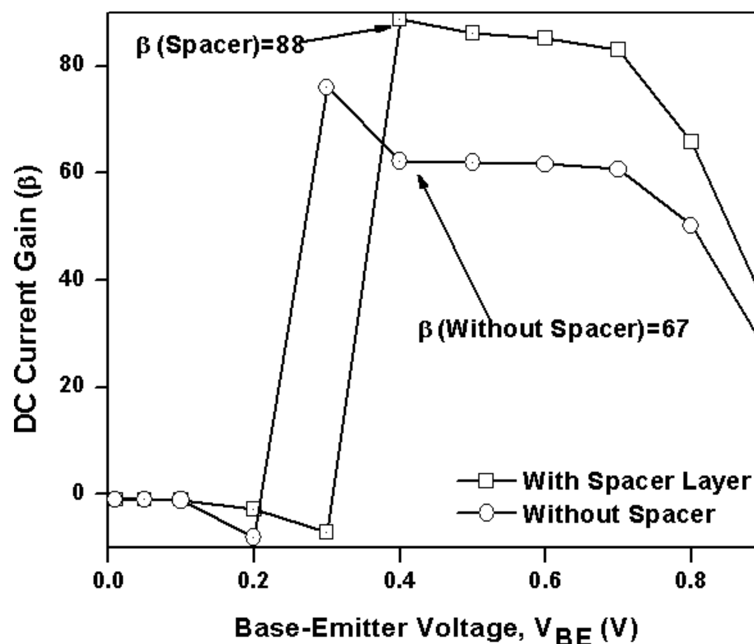

Figure 2: DC current gain of the proposed devices

The I_C versus V_{CE} curves are shown in Figure 3, which reveal a great deal of information on the physics behind the operation of the devices. These curves are plotted for I_B= 5 µA.. It is clear that for the same base current, SiGe HBT with spacer is providing more collector current than other. Such observation is evident in view of the highest β of HBT with spacer.

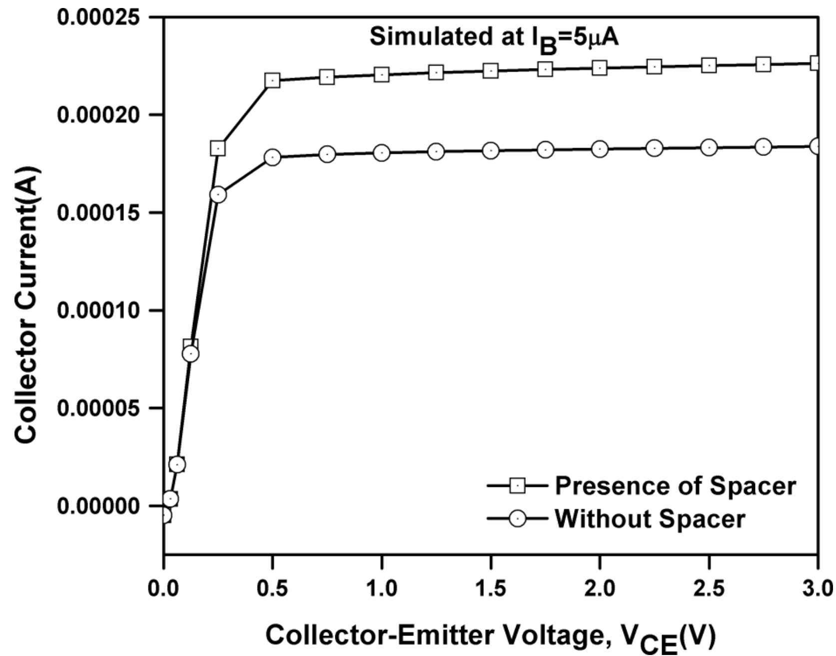

Figure 3: Output Collector-Emitter V_{CE} (V)

The Early voltage (V_A) is computed from backward extrapolated V_{CE}-I_C characteristics shown in Figure 4. The observed Early voltages for HBT with spacer and without spacer are -84 V and -72 V respectively. The V_A is a simple and convenient measure of the output conductance. Higher V_A is desirable for a BJT for better circuit operation. The V_A can be expressed as [9]

$$V_A = \frac{\int_0^{W_B} N_{aB}(\mathrm{x})\,\mathrm{dx}}{N_{aB} W_B \{\frac{\partial W_B}{\partial V_{CB}}\}} = \frac{Q_B(0)}{C_{CB}} \qquad (2)$$

where $Q_B(0)$ is the total base charge at V_{CB}=0 V and C_{CB} is the collector base depletion capacitance.

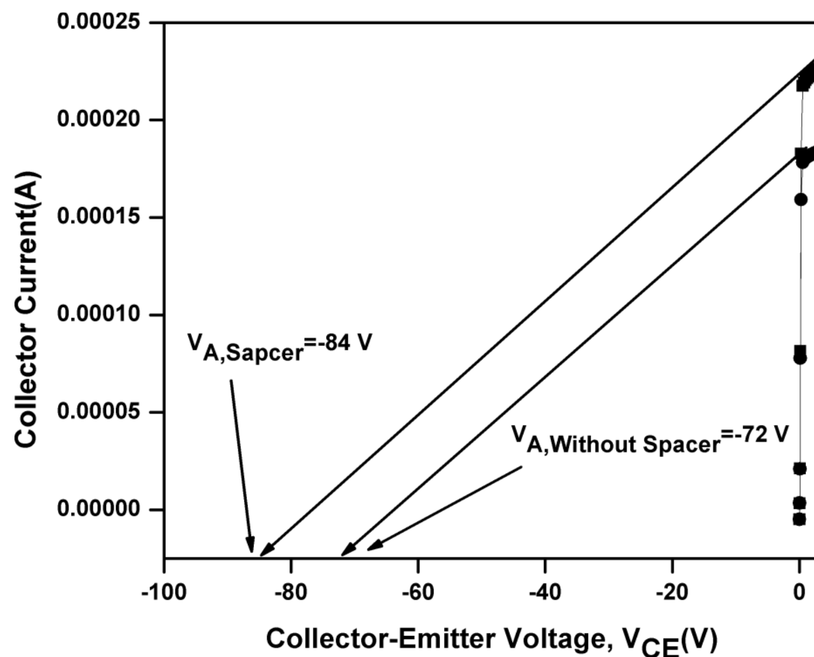

Figure 4: Early voltage V_A (V)

The breakdown voltages in the open base configuration, BV_{CEO} for HBT with the spacer and without spacer are shown in Figure 5. The HBTs are simulated at a base current of, I_B=1e-10 A. The reason for choosing such a small base current is to assume that the base terminal is open. The observed breakdown voltages for the HBTs with the spacer and without spacer are 1.74 V and 1.84 V respectively. The open base configuration BV_{CEO} can be expressed as [10]

$$BV_{CEO} = \frac{BV_{CBO}}{\sqrt[n]{\beta}} \quad (3)$$

where BV_{CBO} is the CB breakdown voltage with the emitter left open. The low breakdown voltage for HBT with spacer can be understood from expression (14), that the high dc current gain of the device is mainly responsible for the lower the break down voltage and vice versa.

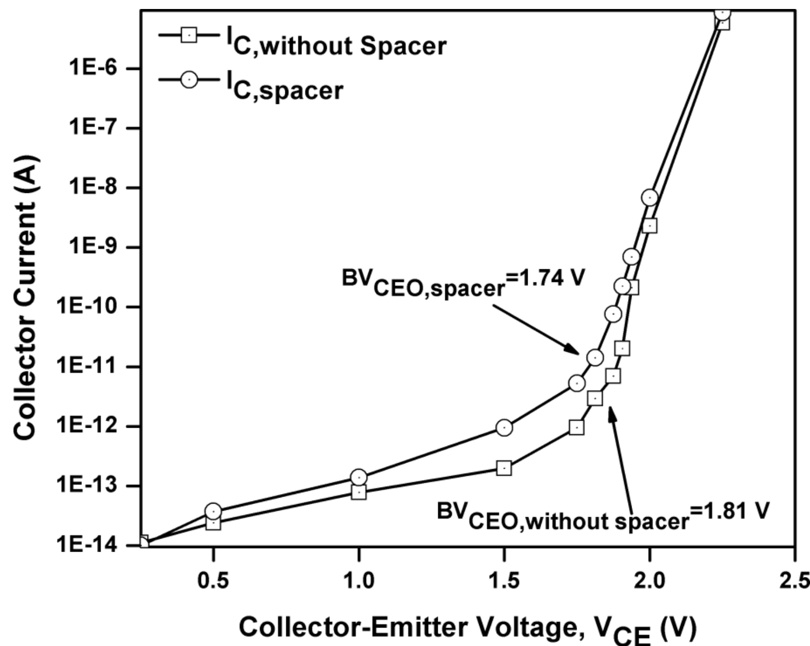

Figure 5: Breakdown Voltage, BV_{CEO} (V)

4.2. RF and Microwave Characteristics:

The RF and Microwave characteristics of the device are studied by AC small-signal analysis using a two-port network [11]. The characteristics analyzed include cut-off frequency (f_t), max frequency of oscillation (f_{max}), Mason's Unilateral Gain (MUG), and stability factor. The input reflection coefficients of the devices are computed from Smith Chart.

The high frequency performance of the simulated bipolar transistors is characterized by 'S' parameters extracted from the Silvaco tool. The cutoff frequency (f_t), defined as the frequency at which the magnitude of short circuit current gain $|h_{21}| = 1$, is plotted in Figure 6. They are recorded to be 40.6 GHz and 16.57 GHz for the SiGe HBT with spacer and without spacer layer respectively. The cut-off frequency (f_t) can be expressed as

$$f_t = \frac{1}{2\pi\tau_b} \quad (4)$$

where τ_b is the base transit time, defined as the time required to discharge the excess minority carriers in the base through the collector current [12]

$$\tau_b = \frac{W_B{}^2}{D_{nB}} \quad (5)$$

where, W_B^2 is the width of base region, D_{nB} is the diffusion coefficient of electrons in the base region. It is observed that the D_n values of the SiGe HBT with spacer is less than that of without spacer. [13] This makes the base transit-time small in HBT with spacer. with the consequence of higher cutoff frequency of the device compared to the others.

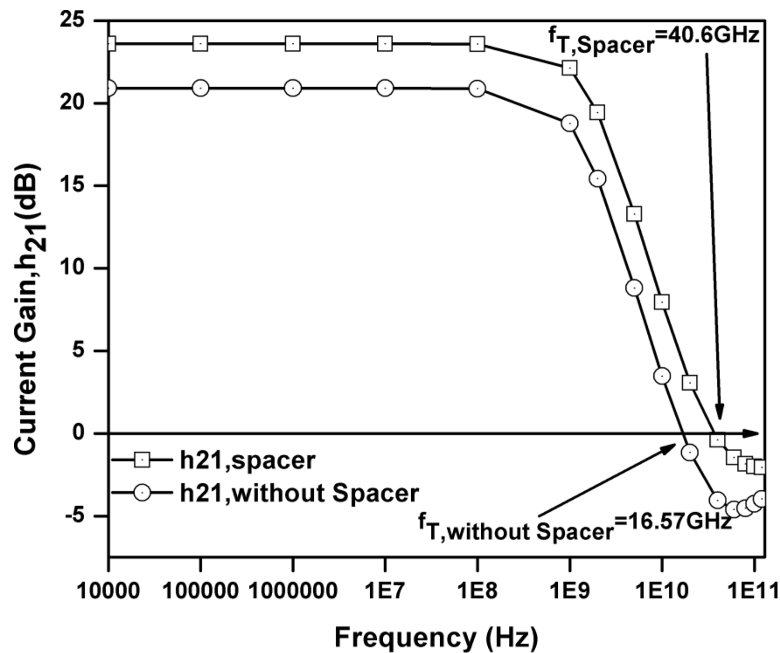

Figure 6: Cut-off frequency, f_T

f_{max} is the maximum oscillation frequency of a device and it is determined with the condition $|MUG| = 1$, using unit-gain-point method. A comparative account of Massion's Unilateral Power Gain plots for all the transistors is presented in Figure 7. The maximum frequencies of oscillation f_{max} of SiGe HBT with spacer and without spacer are found to be 17.58 GHz and 14.33 GHz respectively. The maximum oscillation frequency is expressed as [12]

$$f_{max} = \sqrt{\frac{f_t}{8\pi r_b c_{jc}}} \quad (6)$$

where f_t is cut-off frequency, r_b the base resistance, and c_{jc} is the collector junction capacitance. It is observed that f_{max} is higher as f_t is higher and vice versa. The stability factor, K, measures whether a transistor will be unconditionally stable for arbitrary passive loads [14]. The Rollett stability factor can be expressed in terms of S-parameters as [12]

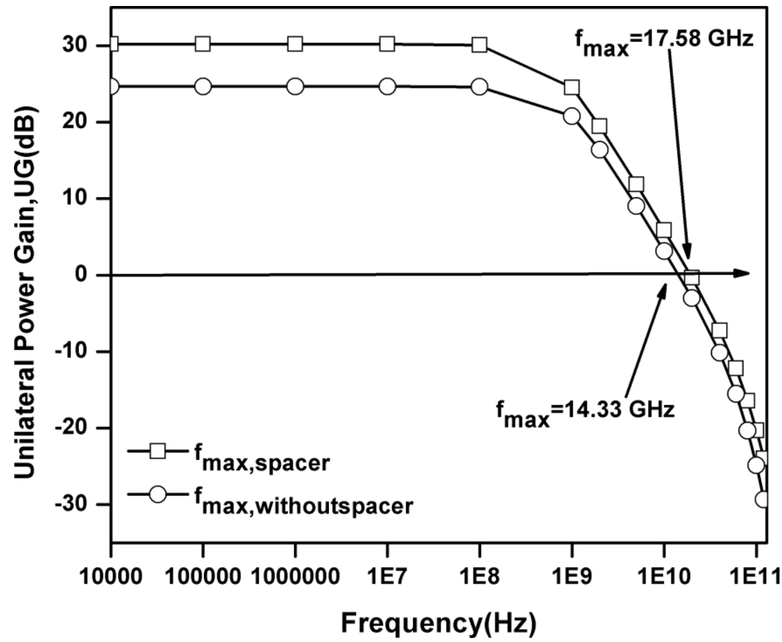

Figure 7: Maximum frequency of oscillation, f_{max}

$$K = \frac{1-|s_{11}|^2 - |s_{22}|^2 + |\Delta s|^2}{2|s_{12}.s_{21}|} \tag{7}$$

where $\Delta s = s_{11}s_{22} - s_{12}s_{21}$. The stability factors of all the transistors are shown in Figure 8. It is observed that the HBT with the spacer is potentially unstable from the frequency 10^7 Hz to 10^9 Hz as K<1, whereas without spacer layer is inherently stable as K>1 for all range of frequency operation.

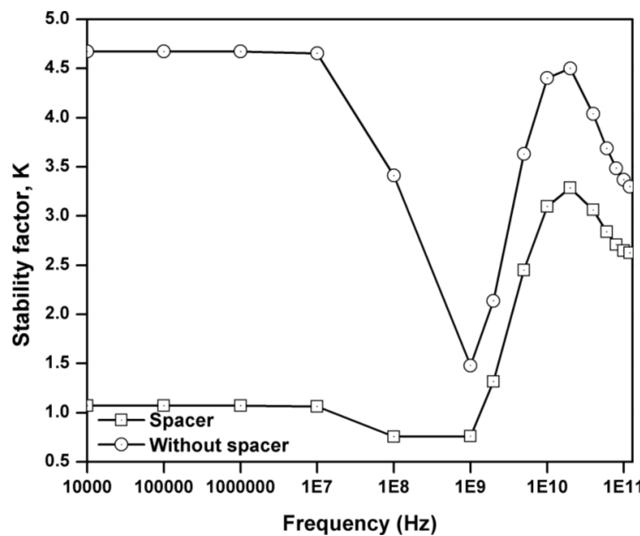

Figure 8: Stability factor, K

The RF parameters S_{11} and S_{22} for the HBTs are computed using Smith Chart in the frequency range from 1 Hz to 120 GHz. Smith Chart helps to determine the device input and output reflection coefficients (Γ). If Γ is less than 0.33, then there is no need of any matching network at the input as well as output side. Mathematically reflection coefficient at the input side is expressed as,

$$\Gamma_{in} = \sqrt{\mathrm{Re}(S_{11})^2 + \mathrm{Im}(S_{11})^2} \tag{8}$$

And at the output side is expressed as

$$\Gamma_{out} = \sqrt{\mathrm{Re}(S_{22})^2 + \mathrm{Im}(S_{22})^2} \quad (9)$$

The reflection coefficient as a function of frequency is plotted in Figure 9. It is clear that at the input site no matching network is required, whereas at the output side matching network is required as reflection coefficient, $\Gamma_{out} > 0.33$ for HBTs.

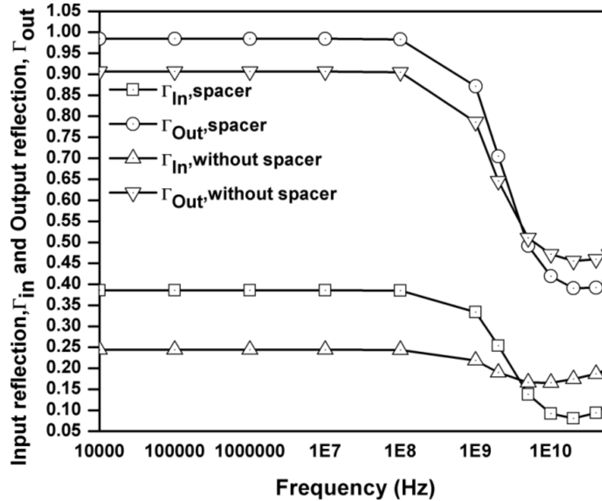

Figure 9: Total reflection coefficients

The minimum noise figures NF_{min} are determined by sweeping the base bias from 0 to 1.25 V and the collector bias from 0 to 2 V keeping the emitter voltage zero. The NF_{min} thus determined for the HBTs are depicted in Figure 10. It may be observed from this figure that, the NF_{min} records constant values 1.9 dB and 2.16 dB respectively upto a frequency of 3.29 GHz. Thereafter, the NF_{min} curves rise steeply to attain some peaks and then fall quickly to low values. Such a behavior of NF_{min} can be understood by writing the theoretical expression as [9]

$$NF_{min} = 1 + \frac{1}{\beta} + \sqrt{2g_m r_b}\sqrt{\frac{1}{\beta} + \left(\frac{f}{f_T}\right)^2} \quad (10)$$

It may be observed from this expression that NF_{min} depends on β and f_t in a critical way. At low frequency (much below f_t), the second term inside the square root becomes negligible. This is manifested in two ways. First, the frequency dependence of NF_{min} vanishes which renders it constant and secondly the dc gain dominates as a reciprocal term, for which the constant values of NF_{min} are observed to be in the reverse order of β values for the HBTs.

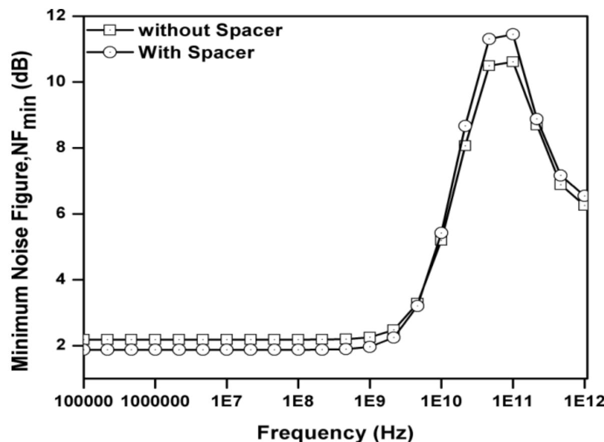

Figure 10: The minimum noise figure, NF_{min} (dB)

5. Conclusion:

The SiGe HBT with spacer and without spacer are studied in this work and an attempt is made to compare, analyse and validate the properties of the HBTs using TCAD Software and simple physics relations within this framework. The HBT having spacer is found to exhibit the higher current gain of 88 compared to the HBT having no spacer layer. The highest cut-off frequency is achieved in the case of HBT with spacer. In general by introducing the spacer layer in SiGe HBT, the device performances are improved in terms of higher V_A, higher f_{max}, and lower minimum noise figure (NF_{min}).

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