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Data Encoding Techniques to Reduce the Switching Activity, Crosstalk Delay Classes and Crosstalk Delay

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Abstract: System on Chip (SoC) has provided many advantages, but also many design challenges. Network on Chip (NoC) has developed to solve the problems associated with communication requirements in SoC. Contribution of power dissipation of communication requirements is much greater than the remaining requirements of the SoC. As technology scales down, interconnects are becoming more power hungry in NoC. The power dissipation of interconnects is directly proportional to switching activity factor of interconnects, capacitance, operating voltage and frequency. Operating voltage, frequency and capacitances are technology dependent. Switching activity is the one, which is technology independent. Switching activity of interconnects only depends on data patterns which are travelling on interconnects. Hence, in this paper an attempt has made to reduce the switching activity of interconnects using data encoding techniques. Moreover, impact of proposed data encoding techniques on crosstalk classes in three wire model has analyzed. Experiments have been carried out with 8-bit, 16-bit, 32-bit and 64-bit data sizes to study the performance of the proposed data encoding techniques. Experimental results show that the proposed data encoding techniques have provided better performance efficiency in all aspects with less area overhead.

Key words: Switching activity, Data encoding, Low power, System on Chip (SoC).

I. INTRODUCTION

Recent trends in ultra deep submicron meter era have resulted in high performance and power efficient logic blocks, but less performed and high power consuming interconnects [13]. In fact, interconnects are consuming 50% of the entire dynamic energy dissipation in recent technologies, and this anticipated to rise to 65%-80% over the following several years [27]. Chip measure remains generally steady in light of the fact that the chip work keeps on expanding and RC delay increments exponentially. SoC design methodologies are providing the ability to integrate many cores in single silicon die as shown in Fig.1, but the same ability of SoC has faced the challenge as to provide the reliable communication among the number of cores [39]. Network on Chip (NoC) is rising as a layout paradigm to deal with the scalability and reliability troubles of SoC [4].

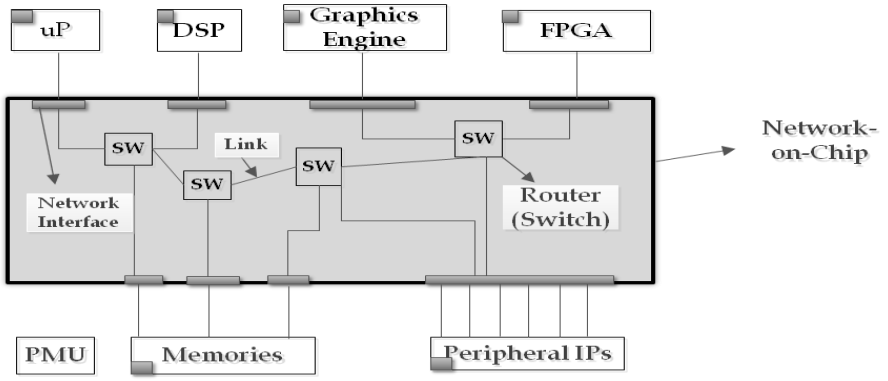

Fig.1 System on Chip (SoC)

In recent times, the on-chip communication problems are much dominating than the computational associated problems [4]. In fact, the communication subsystem increasingly more influences the conventional design goals, along with cost, performance, power dissipation, and reliability. As technology shrinks, power consumption of communication subsystem is much dominating than the power consumption of remaining requirements in SoC.

In this paper, we present a set of data encoding techniques working at flit level, which permits us to limit both the self and coupling switching activity on interconnects of the routing paths [17]. The

proposed data encoding techniques are obvious to router implementation. Moreover, data encoding techniques have assessed by using simulation on various flit sizes. The evaluation takes into consideration numerous factors and metrics of the design, including overhead area and delay of proposed data encoding techniques, efficiency in terms of switching activity, energy consumption, and delay of interconnects. The outcome shows that the proposed data encoding techniques have provided better performance.

The rest of this paper has prepared as follows. The associated works are discussed in section II, while section III provides detailed description of the proposed data encoding techniques. In section IV, the results are presented and performance of proposed data encoding techniques has compared with different techniques. Eventually, this paper has concluded in section V.

II. RELATED WORKS AND CONTRIBUTIONS

Within the coming few years, we may expect that thousand number of cores integrated in SoC [41]. In these SoCs, a major fraction of the total system power dissipation is due to interconnects which are used to connect the cores in SoC as shown in Fig.1. Hence, most of the research work which published in literature has aimed to reduce the power dissipation due to interconnects. Due to the fact that the point of interest of this paper is on lowering the power dissipated by interconnects. Number of the works which are aimed to reduce the interconnect power are described here. These encompass the strategies that employ shielding [23], [11], growing line-to-line spacing [20], [1], and repeater insertion [3] which is increases the overall area of chip. Another approach to reduce the power dissipation of interconnects is data encoding techniques. One category of data encoding techniques is aimed to reduce the power dissipation due to self switching activity by ignoring the coupling switching activity. In this category, bus invert (BI) [35] and INC-XOR [28] had been proposed for the case that random data patterns are transmitted via interconnects. Whereas gray code [36], T0 [5], working-zone encoding [14], and T0-XOR [10] have suggested within the case of correlated data styles. Application-specific techniques have additionally been proposed in [6], [7], [2], [21], [43]. But, this category of encoding is not always continually suitable especially in the deep sub micron meter technology wherein the coupling capacitance is dominating. Hence power consumption due to coupling switching activity has major contribution in total power consumption. Data encoding techniques which ignore the effect of the coupling switching activity is in advocate to analyze the power consumption of interconnects [25]. The works within another category of data encoding techniques are aimed to limit the power dissipation due the coupling switching activity [1], [43], [25], [19], [26], [16], [29], [15], [42], [9]. Among those schemes, [1], [19], [26], [16], [29], [15], are reduces switching activity by introducing the extra control lines. The strategies proposed in [42] and [9] have used less control lines with more complex decoding logic. The scheme presented in [16] aimed to decrees the coupling switching. In this approach, a complicated data encoder estimate the Type-I and Type-II coupling switching activity with weighting coefficients as 1 and 2 respectively and from that total coupling switching activity is estimated. If the total coupling switching activity is greater than the half of the data size, then the inversion can do. Further to the complicated encoder, the approach most effective works at the patterns whose full inversion results in the link power reduction at the same time as not thinking about the patterns whose full inversions may additionally cause higher link power consumption. Consequently, the link power reduction done through this approach is not always as large as it is able to be. This scheme has based totally at the hop-by-hop approach. The scheme presented in [30] has calculated hamming distance between present and past odd/even data bits and based on hamming distance it performed data inversion to reduce the switching activity. In [26], every bunch of 4 bits are represented with 5 bits and shielding wires are inserted in modified bits to avoid the patterns “101” and “010”. This technique successfully reduces the Type-II coupling switching activity from that it reduces power consumption significantly but increases the transit delay and communication traffic because of using the extra bits. Data encoding technique which proposed in [25] is aimed to reduce the only Type-II coupling switching activity. In [24], three data encoding techniques have presented based on power models of normal data, odd inverted data, even inverted data and fully inverted data.

Coupling capacitance not only provides coupling switching activity, but also provides Crosstalk. Crosstalk reduces the reliability of the communication subsystem of SoC.Wameedh N. Flayyih et al. [38] have provided Crosstalk-Aware Multiple Error Detection Scheme Based on Two-Dimensional Parities for Energy Efficient Network on Chip and overhead power, area and delay have been reduced by using pass transistor logic [8]. Neel Gala et al. [23] have presented Approximate Error Detection with Stochastic Checkers. Jiaqiang Li et al. [22] presented Extending 3-bit Burst Error-Correction Codes With Quadruple Adjacent Error Correction to address the reliability of system on chip. Guoyue Jiang et al. [18] have presented a novel scheme to reduce the latency and power of system on chip. Xiaokun Yang et al. [40] have proposed a high performance on chip bus to meet dynamic energy efficiency. Mohamed S. Abdelfattah et al. [21] have presented embedding

network on chip on FPGA to implement system level communication. SundarrajanRangachari et al. [33] have reduced the dynamic power by adding the bias.

In this paper, we proposed three data encoding schemes which are named as Normal/Odd inversion by considering the Self and Coupling transitions (NOSC), Full/Normal/Odd inversion by considering the self and coupling transitions (FNOSC) and Odd/Even/Full/Normal inversion by considering the Self and Coupling transitions (OEFNSC).

III. PROPOSED ENCODING SCHEMES

In this section, we have discussed about overview of proposed data encoding techniques, introduction of cross-talk delay classes in three wire model and finally, detailed description of proposed data encoding techniques which are aimed to reduce the self and coupling switching activity of interconnects.

3.1 Overview of the proposed data encoding techniques

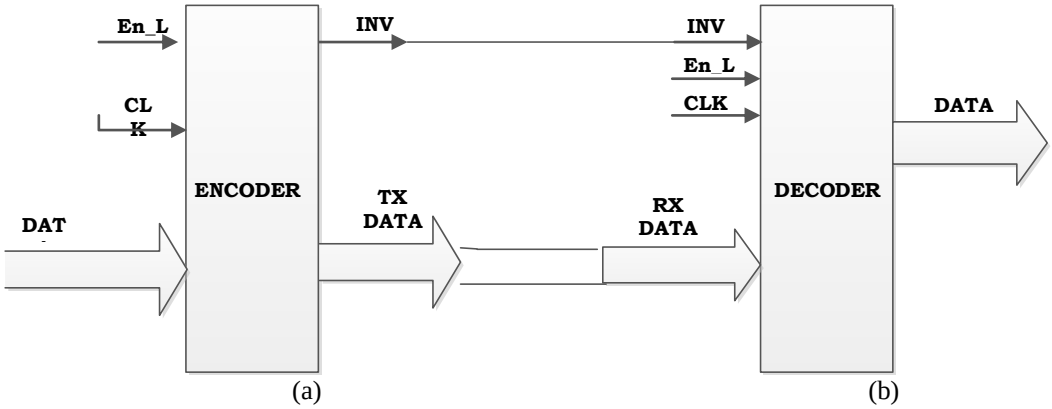

Fig.2 (a) Encoder (b) Decoder

Self and Coupling switching activities are the main source for power consumption of interconnects. Therefore, proposed data encoding techniques have aimed to minimize both the self and coupling activity factors. Fig.2 shows the general encoder/decoder blocks which are incorporated at network interface in Network-on-Chip. The dynamic power dissipation by the interconnects is given by

$$P_{dyn} = \frac{1}{2}\{\alpha_S (C_S + C_L) + \alpha_C C_C\} * V_{DD}^2 * F_{CLK} \quad (1)$$

Where α_S : self switching activity , α_C : coupling switching activity , C_S : substrate capacitance , C_L : load capacitance, C_C : coupling capacitance between two adjacent interconnects, V_{DD} : supply voltage , and F_{CLK} : operating clock frequency. Here, three schemes named as Normal/Odd inversion by considering the self and coupling transitions (NOSC), Full/Normal/Odd inversion by considering the self and coupling transitions (FNOSC) and Odd/Even/Full/Normal inversion by considering the self and coupling transitions (OEFNSC).

3.2 Cross-talk Classes and Cross-talk Delay

One of the important effects of coupling capacitances is Crosstalk. In two or three wire models, wires are termed as *aggressor* and *victim*. Switching transition on *aggressor* wire has produced noise spike in *victim* which is adjacent to *aggressor* wire. Coupling capacitance has dominating factor than self capacitance due to short distance between *aggressor* and *victim*. Consequently, a switching transition in aggressor interconnect produces massive inadvertent spike at the victim even no switching transition at victim which resulting in malfunction on victim interconnect and improved delay because of unwanted charging phase and discharging phase. Sotiriadis et al. [34] has proposed a delay model for three wire model. Based on delay model, crosstalk has categorized as 1C, 2C, 3C, 4C, 5C and 6C. Table-1 has provided the cross-talk classes and delay normalized to $C_L R_W$ [12] [31].

Table-1: Crosstalk Classes and their delays

Crosstalk Classes	Transition Patterns	Relative delay on middle interconnect
1	---,--↑,↑--,--↓,↓--,↑-↑,↑-↓,↓-↑	0
2	↑↑↑,↓↓↓	C_LR_W
3	-↑↑,↑↑-,-↓↓,↓↓-	$C_LR_W(1+\lambda)$
4	-↑-,-↓-,↓↓↑,↑↓↓,↑↑↓,↓↑↑	$C_LR_W(1+2\lambda)$
5	-↑↓,-↓↑,↓↑-,↑↓-	$C_LR_W(1+3\lambda)$
6	↓↑↓,↑↓↑	$C_LR_W(1+4\lambda)$

3.3 NOSC data encoding technique

In this proposed scheme, first we calculated self transitions, and coupling transitions in two possible ways: i) between normal data to be transmit and data which is travel on interconnects ii) between odd positional inverted data which is to be transmitted and data which is travelling on interconnects. Total switching activity (sum of self and coupling switching activities) has estimated in two possibilities and finally data which provides less total switching activity has transmitted. NOSC data encoder produce signal 'INV' to convey the type of the inversion done by the encoder to the decoder to reconstruct the original data. The decoder has tested the 'INV' signal, if INV = '0', then decoder accepts the data as it is, if INV = '1', then decoder is first inverted the received data in odd positions and accepted.

3.4 FNOSC data encoding technique

In this proposed scheme, first we calculated self transitions, and coupling transitions in three possible ways: i) between normal data to be transmitted and data which is travelling on interconnects ii) between odd positional inverted data which is to be transmit and data which is travel on interconnects iii) between fully inverted data to be transmit and data which is travel on interconnects. Total switching activity (sum of self and coupling switching activities) has estimated in three possibilities and finally data which provides less total switching activity has transmitted. FNOSC data encoder produce signal 'INV' to convey the type of the inversion done by the encoder to the decoder to reconstruct the original data. The decoder has tested the 'INV' signal, if INV = "00", then decoder has accepted the data as it is, if INV = "01", then decoder is first inverted the received data in odd positions and accepted, if INV = "11", then decoder is first inverted the received data and accepted.

3.5 OEFNSC data encoding technique

In this proposed scheme, first we calculated self transitions, and coupling transitions in four possible ways: i) between normal data to be transmit and data which is travel on interconnects ii) between data is inverted only in odd positions which is to be transmit and data which is travel on interconnects iii) between data is inverted only in even positions which is to be transmit and data which is travel on interconnects iv) between fully inverted data to be transmit and data which is travel on interconnects. Total switching activity has estimated in four possibilities and finally data, which provides less total switching activity, has transmitted. OEFNSC data encoder produce signal 'INV' to convey the type of the inversion done by the encoder to the decoder to reconstruct the original data. Initially, decoder has tested the 'INV' signal. If INV = "00", then decoder is accepted the data as it is, if INV = "01", then decoder is first inverted the received data in odd positions and accepted, if INV = "10", then decoder is first inverted the received data in even positions and accepted, if INV = "11", then decoder is first inverted the received data and accepted.

IV. RESULTS AND DISCUSSION

In this section, efficiency of proposed data encoding schemes has analysed in terms of self switching activity, coupling switching activity, crosstalk classes, energy consumption and delay of interconnects in 45nm. 10000 random input vectors with different data sizes as 8-bit, 16-bit, 32-bit and 64bit are considered to analyze the performance of proposed data encoding techniques. Moreover, these data encoding techniques have synthesized using Spartan-3, XC3S15000 FPGA with package FG320.

Table 2 self and coupling transition counts for 10000 random input vectors.

METHOD	Self switching activity				Coupling switching activity			
	8-BIT	16-BIT	32-BIT	64-BIT	8-BIT	16-BIT	32-BIT	64-BIT
UNCODED	21841	39026	75097	147492	73284	131647	272743	527960
SCH-1	19681	38113	69016	144877	49126	107837	212725	440957
SCH-2	15115	34027	70733	143740	42584	102727	225241	445342
SCH-3	18289	36223	72273	147684	30210	84328	170572	339761
NOSC	19717	36662	66762	141588	34393	83204	191965	363868
FNOSC	16712	31951	66110	140128	26099	77426	188027	354198
OEFNSC	10659	29795	63672	136956	20235	70383	168675	333226

Table 2 shows the counts of self transitions and coupling transitions, Table 3 shows the counts of crosstalk class-6 and crosstalk class-5, Table 4 shows the counts of crosstalk class-4 and crosstalk class-3 and Table 5 shows the counts of crosstalk class-2 and crosstalk class-1 for 10000 input vectors with different data sizes.Fig.3. describes the efficiency of data encoding techniques in terms of self switching activity reduction and coupling switching activity reduction. NOSC data encoding technique has given better results compared to SCH-1. FNOSC data encoding technique has given better results compared to SCH-1 and SCH-2. OEFNSC data encoding technique has given self switching activity reduction as 51.2% for 8-bit, 23.66% for 16-bit, 15.22% for 32-bit and 7.15% for 64-bit and it also given coupling switching activity reduction efficiency as 72.39% for 8-bit, 46.54% for 16-bit, 38.16% for 32-bit and 36.89% for 64-bit. From the results, OEFNSC has given better switching activity reduction efficiency.

Table 3 crosstalk class-6 and crosstalk class-5 counts for 10000 random input vectors.

METHOD	Crosstalk class-6				Crosstalk class-5			
	8-BIT	16-BIT	32-BIT	64-BIT	8-BIT	16-BIT	32-BIT	64-BIT
UNCODED	14844	13667	30712	62560	14092	30117	52408	101525
SCH-1	929	2405	8868	22881	5769	17743	34782	65427
SCH-2	1226	2701	9271	25263	6586	18982	36446	66560
SCH-3	549	1996	2915	7683	3324	12164	18743	32468
NOSC	1003	1987	8057	13851	1838	8853	27207	42218
FNOSC	318	2058	7740	12688	1597	9637	28735	41805
OEFNSC	54	1162	2697	8690	581	6839	21768	34795

Table 4 crosstalk class-4 and crosstalk class-3 counts for 10000 random input vectors.

METHOD	Crosstalk class-4				Crosstalk class-3			
	8-BIT	16-BIT	32-BIT	64-BIT	8-BIT	16-BIT	32-BIT	64-BIT
UNCODED	5353	18542	48816	91597	265	5246	9958	26461
SCH-1	12368	24424	50553	107655	6438	17206	25946	61853
SCH-2	8464	22026	49605	106389	3270	12147	22085	59744
SCH-3	4774	17167	42162	88522	9046	20461	44381	95525
NOSC	7959	18647	44195	90330	10484	23592	31907	83313
FNOSC	5023	16345	41776	87686	9348	19511	30378	82244
OEFNSC	3184	14353	40947	82913	7558	22479	37120	89748

Table 5 crosstalk class-2 and crosstalk class-1 counts for 10000 random input vectors.

METHOD	Crosstalk class-2				Crosstalk class-1			
	8-BIT	16-BIT	32-BIT	64-BIT	8-BIT	16-BIT	32-BIT	64-BIT
UNCODED	27	701	1375	4936	25419	71727	156731	332921
SCH-1	3813	4663	7616	22292	30683	73559	172235	339892
SCH-2	817	2589	3950	20133	39637	81555	178643	341911
SCH-3	9976	10932	27107	62670	32331	77280	164692	333132
NOSC	9792	10117	12793	45699	28924	76804	175841	344589
FNOSC	9849	8559	14489	48039	33865	83890	176882	347538
OEFNSC	1968	6647	16358	48742	46655	88520	181110	355112

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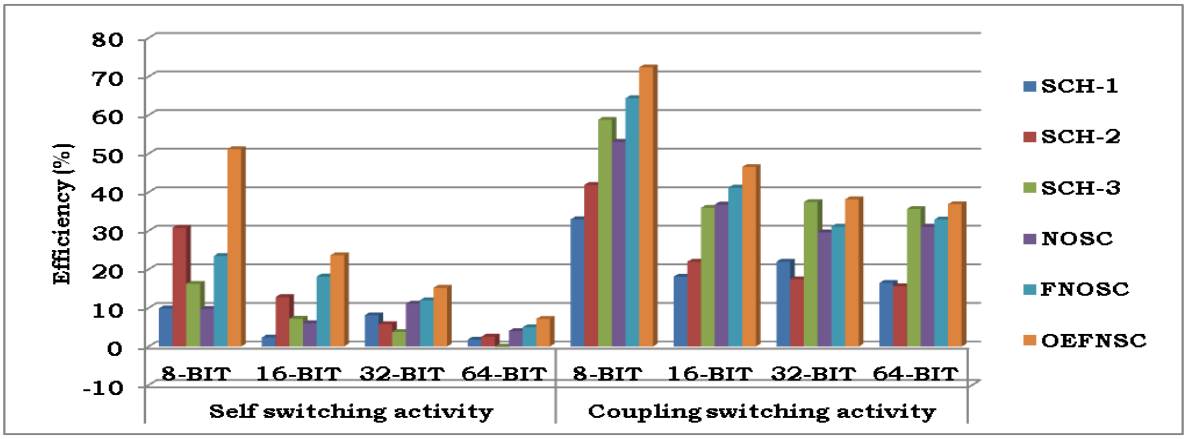

Fig.3. Efficiency of data encoding techniques in terms of self and coupling switching activity.

Fig.4. describes the reduction efficiency of data encoding techniques in terms of crosstalk delay class-6, class-5 and class-4. NOSC data encoding technique has given better results compared to SCH-1. FNOSC data encoding technique has given better results compare to SCH-1 and SCH-2. OEFNSC data encoding technique has given reduction efficiency of crosstalk delay class-6 as 99.64% for 8-bit, 91.5% for 16-bit, 91.22% for 32-bit and 86.11% for 64-bit. OEFNSC data encoding technique has given reduction efficiency of class-5 as 95.88% for 8-bit, 77.3% for 16-bit, 58.47% for 32-bit and 65.73% for 64-bit. OEFNSC data encoding technique has given reduction efficiency of crosstalk delay class-4 as 40.52% for 8-bit, 22.6% for 16-bit, 16.12% for 32-bit and 9.49% for 64-bit. From the results, OEFNSC has given better reduction efficiency in terms of crosstalk delay class-6, class-5 and class-4. Fig.5. describes the reduction efficiency of data encoding techniques in terms of crosstalk delay class-3, class-2 and class-1. Proposed data encoding techniques has increased counts of crosstalk delay class-3, class-2 and class-1 where crosstalk delay class-3, class-2 and class-1 has weight $(1+\lambda)$, '1' and '0' respectively which are much smaller than the weights of crosstalk class-6, class-5 and class-4. Hence, delay efficiency of interconnects has improved by the proposed data encoding techniques even the crosstalk class-3, class-2 and class-1 are increased. Fig.6. describes the efficiency of data encoding techniques in terms of energy consumption and delay of interconnects.

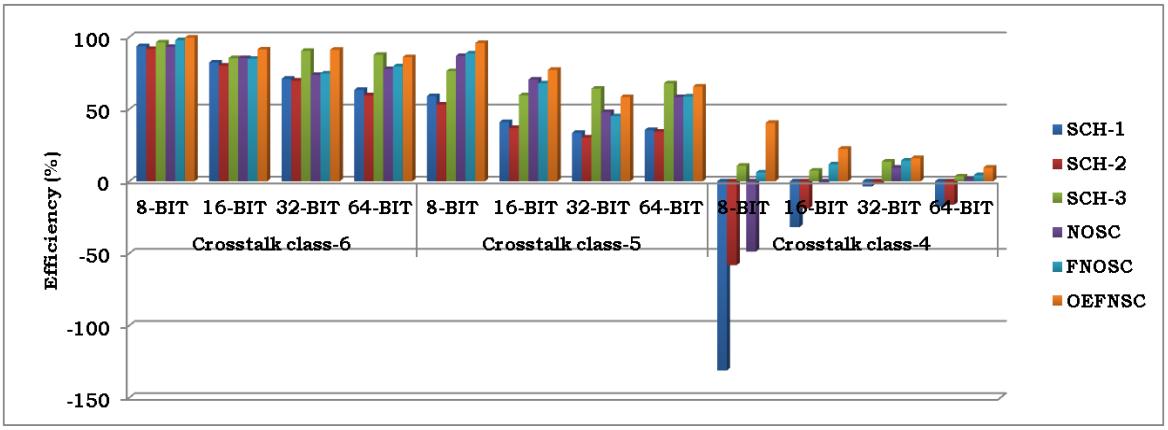

Fig.4. Efficiency of data encoding techniques in terms of crosstalk delay class-6, class-5 and class-4.

NOSC data encoding technique has given energy efficiency of interconnects as 43.12% for 8-bit, 29.77% for 16-bit, 25.62% for 32-bit and 25.17% for 64-bit. FNOSC data encoding technique has given energy efficiency of interconnects as 55% for 8-bit, 35.92% for 16-bit, 26.94% for 32-bit and 26.82% for 64-bit. OEFNSC data encoding technique has given energy efficiency of interconnects as 67.53% for 8-bit, 41.31% for 16-bit, 33.21% for 32-bit and 30.4% for 64-bit.

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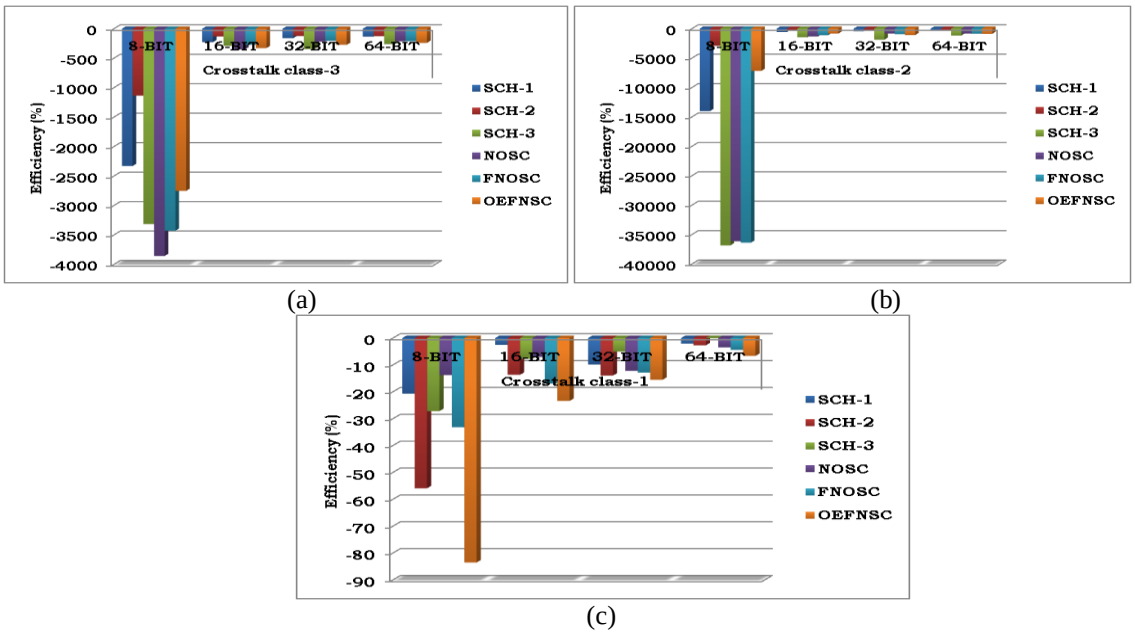

Fig.5. Efficiency of data encoding techniques in terms of (a) crosstalk delay class-3 (b) crosstalk delay class-2 and (c) crosstalk delay class-1.

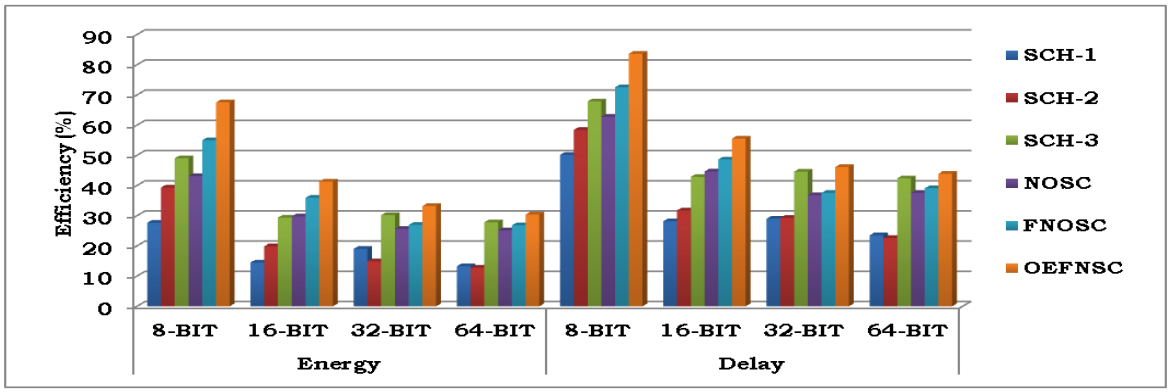

Fig.6. Efficiency of data encoding techniques in terms of Energy and Delay.

NOSC data encoding technique has given delay efficiency of interconnects as 62.8% for 8-bit, 44.64% for 16-bit, 36.77% for 32-bit and 37.54% for 64-bit. FNOSC data encoding technique has given delay efficiency of interconnects as 72.56% for 8-bit, 48.63% for 16-bit, 37.55% for 32-bit and 39.08 for 64-bit. OEFNSC data encoding technique has given delay efficiency of interconnects as 83.66% for 8-bit, 55.55% for 16-bit, 46.15% for 32-bit and 43.92% for 64-bit. Synthesis report of the proposed data encoding techniques has summarized in Table 6, Table 7, Table 8, and Table 9. Synthesis report describes the overhead of the proposed data encoder/decoder. From the all results, NOSC data encoding technique has provided better performance than the Scheme-1 [24], FNOSC data encoding technique has provided better performance than the Scheme-2 [24] and OEFNSC data encoding technique has provided better performance than the Scheme-3 [24]. Among the six data encoding techniques, OEFNSC provided better performance in all aspects.

Table 6 Synthesis report of Data encoding schemes for 8-bit data

Data Encoding	ENCODER					DECODER				
	SLICES	LUT	DELAY(ns)			SLICES	LUT	DELAY(ns)		
			Total Delay	Logic	Route			Total Delay	Logic	Route
SCH-1	97	189	14.1	6.13	7.97	4	8	7.99	6.1	1.89
SCH-2	99	193	16.28	6.51	9.77	6	11	4.09	1.85	2.24
SCH-3	177	348	18.92	7.11	11.82	5	9	9.29	6.58	2.71
NOSC	25	48	9.77	4.24	5.52	4	8	7.99	6.1	1.89
FNOSC	71	137	15.16	6.55	8.61	6	11	4.09	1.85	2.24
OEFNSC	138	267	18.57	7.15	11.43	5	9	9.29	6.58	2.71

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Table 7 Synthesis report of Data encoding schemes for 16-bit data

Data Encoding	ENCODER					DECODER				
	SLICES	LUT	DELAY(ns)			SLICES	LUT	DELAY(ns)		
			Total Delay	Logic	Route			Total Delay	Logic	Route
SCH-1	187	370	18.56	7.34	11.22	9	16	8.13	6.1	2.03
SCH-2	262	508	21.9	9.12	12.77	11	19	4.33	1.85	2.48
SCH-3	466	906	25.48	10.88	14.59	10	17	9.73	6.58	3.15
NOSC	111	214	16.67	6.47	10.19	9	16	8.13	6.1	2.03
FNOSC	143	280	19.43	8.04	11.39	11	19	4.33	1.85	2.48
OEFNSC	329	637	23.01	8.46	14.55	10	17	9.73	6.58	3.15

Table 8 Synthesis report of Data encoding schemes for 32-bit data

Data Encoding	ENCODER					DECODER				
	SLICES	LUT	DELAY(ns)			SLICES	LUT	DELAY(ns)		
			Total Delay	Logic	Route			Total Delay	Logic	Route
SCH-1	398	779	39.49	20.34	19.15	18	32	8.65	6.1	2.55
SCH-2	827	1601	32.18	13.11	19.07	21	37	4.14	1.85	2.29
SCH-3	1488	2896	32.39	13.34	19.05	19	33	9.81	6.58	3.23
NOSC	281	544	22.9	9.03	13.87	18	32	8.65	6.1	2.55
FNOSC	458	895	27.4	10.38	17.02	21	37	4.14	1.85	2.29
OEFNSC	1004	1963	30.22	11.77	18.45	19	33	9.81	6.58	3.23

Table 9 Synthesis report of Data encoding schemes for 64-bit data

Data Encoding	ENCODER					DECODER				
	SLICES	LUT	DELAY(ns)			SLICES	LUT	DELAY(ns)		
			Total Delay	Logic	Route			Total Delay	Logic	Route
SCH-1	1049	2055	79.44	41.23	38.21	37	64	8.81	6.1	2.71
SCH-2	2810	5486	43.31	16.21	27.1	40	69	4.67	1.85	2.82
SCH-3	3876	7594	49.48	19.34	30.15	37	65	10.77	6.58	4.19
NOSC	910	1778	40.38	15.73	24.65	37	64	8.8	6.1	2.71
FNOSC	1004	1957	49.5	23.16	26.34	40	69	4.67	1.85	2.82
OEFNSC	1950	3798	39.5	15.76	23.75	37	65	10.77	6.58	4.19

V. CONCLUSIONS

In this paper, proposed data encoding techniques are independent of type of interconnect used and application handled of communication subsystem in SoC. Hence, these data encoding techniques are applicable to any type of interconnects to reduce the dynamic power dissipation of interconnects. The proposed data encoding techniques has reduced not only the self switching activity, but also the coupling switching activity that is especially liable for link energy dissipation in the deep sub micron meter technology regime. Moreover, in literature most of the data encoding techniques have aimed to reduce only switching activity or crosstalk delay classes. An extensive assessment has accomplished to evaluate the impact of proposed data encoding schemes in terms of self switching activity, coupling switching activity, crosstalk delay classes, energy consumption of interconnects and delay of interconnects. Proposed data encoding techniques have provided better performance in all aspects with slight penalty of overhead.

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