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Effect Of Semiconducting Purity Of Single-Walled Carbon Nanotubes On The Electrical Performance Of Flexible Carbon Nanotube Thin Film Transistors

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Abstract: This paper reports the fabrication of bottom-gate carbon nanotube thin film transistors (CNTTFTs) of varying dimensions on a flexible polyimide substrate using 99.99% and 95% semiconducting purity single-walled carbon nanotubes (SWCNTs) for the formation of channel thin film and their electrical performance study at room temperature. The CNTTFTs uses hafnium dioxide(HfO_2) as high dielectric constant gate dielectrics. The devices exhibited p-type behavior in both the cases of CNTTFTs with 99.99% and 95% semiconducting purity SWCNTs used for fabrication. The flexible CNTTFT with 99.99% semiconducting purity SWCNTs of channel length(L) =50µm, width (W)=50 µm has exhibited an on-current of 2.33mA, on/off current ratio of $1.39X10^4$, a mobility of 4.68 cm^2/Vs, the transconductance of 45.7 µS and a subthreshold swing of 716.94mV/decade. The CNTTFT of L=50 µm, W=50 µm with 95% semiconducting purity SWCNTs has exhibited an on-current of 2.33mA, on/off current ratio of 1.3 $X10^3$, a mobility of 4.61cm^2/Vs, the transconductance of 43 µS and a subthreshold swing of 933 mV/decade. This work demonstrated that the flexible CNTTFTs which used 99.99% semiconducting purity SWCNTs outperforms the flexible CNTTFTs which used 95% semiconducting purity SWCNTs and have exhibited higher on/off current ratio, mobility, transconductance, and lower subthreshold swing. This work also demonstrates that for the better electrical performance of flexible CNTTFTs should have SWCNTs of higher semiconducting purity and density.
Keywords: carbon nanotubes, carbon nanotube thin film transistors, channel, mobility, on/off current ratio.

1. Introduction

Nowadays flexible applications, for example, integrated circuits, e-paper, electronic tags, artificial skin, wearable displays, sensors, digital circuits, fingerprint scanners are implemented using carbon nanotube thin film transistors (CNTTFTs) are demonstrated in the works [1-7]. The thin-film of single-walled carbon nanotubes (SWCNTs) is used as the channel materials for the fabrication of CNTTFTs on flexible substrates are demonstrated in the works [1-7]. SWCNTs have the advantages of their extremely good electrical and mechanical bendable properties [8-11]. But other channel materials amorphous and organic semiconductors have low mobilities and only used for low -frequency applications [12-14]. The electrical parameters such as maximum on current, on current density, on-off current ratio, subthreshold swing, mobility, transconductance of CNTTFTs on rigid and flexible substrates are extracted to decide the performance of CNTTFTs [3,6,8,15,16,17]. Based on these parameters the feasibility of the devices to be used for the practical flexible electronics applications is decided. Mainly the important electrical parameters of CNTTFTs are on-off current ratio,mobility and on current density. These parameters can be improved by the considering the type of the flexible substrate, the density of the SWCNTs deposited in the channel area,orientation of the nanotubes (aligned or random network) [18,19,20,21,22,23,24,25], semiconducting purity of the SWCNTs,the type,thickness and process used for deposition of gate dielectric, the metals used for the formation of source, drain and gate electrodes [3,6,7,8,10,16,17]. The current work focus on the fabrication of CNTTFTs using varying semiconducting purity SWCNTs solutions of 99.99% and 95% for the channel thin film development and electrical parameters are studied with varying length and width of the devices. The electrical parameters are also compared with the similar works appeared in the literature.

2. Devices fabrication

In this work, the fabrication of bottom-gate CNTTFTs with photolithography steps were used for patterning of the source, drain and gate electrode, and SWCNTs thin film formation. The SWCNTs thinfilm was deposited by immersion method on aminoisopropyl triethoxysilane (APTES) [18,19,20] functionalized HfO_2 surface. Procedural steps for fabrication of bottom-gate CNTTFTs are shown in figure1.

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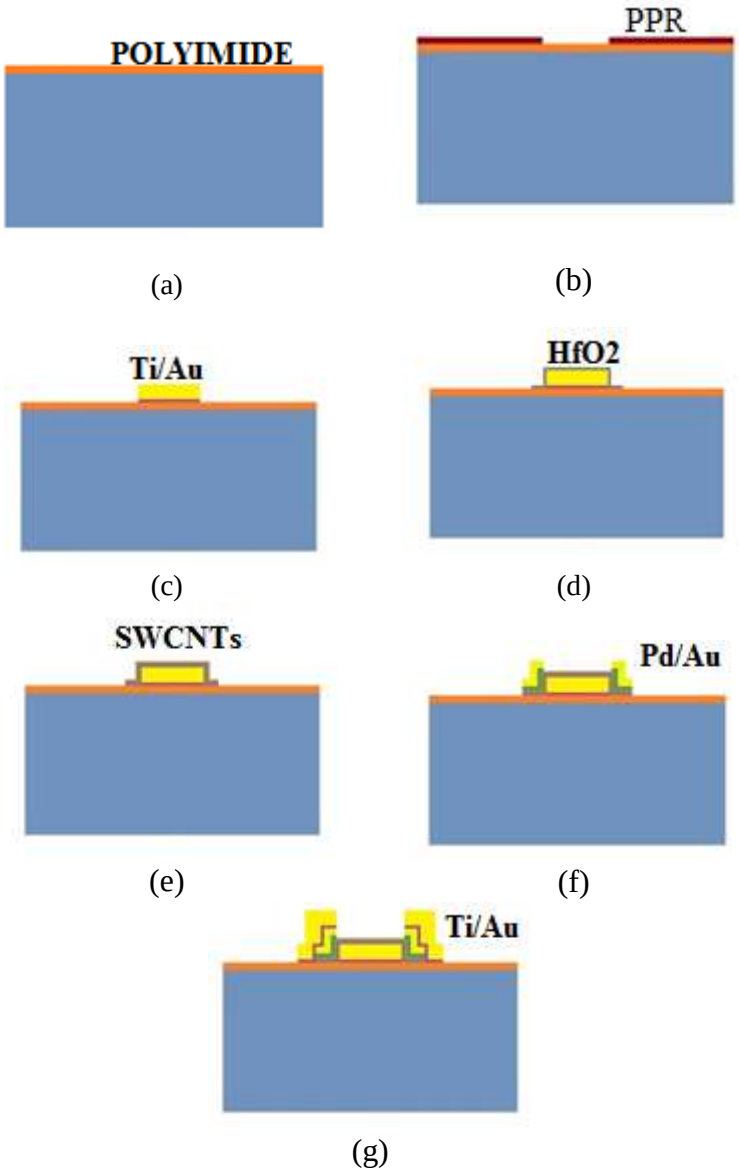

Figure1. Procedural steps for fabrication of bottom-gate CNTTFTs (a) Polyimide substrate pasted on the Si wafer. (b) Patterned PPR layer. (c) Patterned Ti/Au gate. (d) Patterned gate dielectric HfO_2. (e) Patterned SWCNTs deposited on HfO_2 surface. (f) Patterned Pd/Au the source and drain electrodes. (g) Patterned Ti/ Au for large area source, drain, gate contact pads.

The GDSII format of the Clewin layout was used by the laser writer LW 405 to edit masks on iron-oxide coated plates. The flexible polyimide tape 5413M with silicone adhesive of the width 25.4mm, length of 40 mm and a thickness 75µm was pasted on the 2 inch Si wafer is shown in the figure1(a). The polyimide substrate fixed on the Si wafer was preheated at 90^{o}C for 5 minutes prior to the lithography process. The photolithography wascarried out by double-sided aligner DSA EVG 620. The developed PPR patterned for bottom-gate is as seen in figure 1(b). The patterning of the metal titanium/gold (Ti/Au) for the gate was done by photolithography procedure. The bottom-gate metal titanium/gold (Ti/Au) of thickness 10/50nm was deposited by 4-target E-beam evaporator (4-TEBE) and patterned using photolithography is as seen in figure 1(c). Subsequently, the deposition of gate dielectric HfO_2 of thickness 10nm was done by RF sputtering and patterned using photolithography is as seen in figure 1(d). The deposition of SWCNTs on the HfO_2 layer after the APTES functionalization of dielectric was done to rise the density of the nanotubes deposited. The 95% semiconducting purity SWCNTs solution was procured from the Nano Integris Inc., USA. The solution obtained was in the form of a solvent-surfactant solution with a concentration of 1.0 mg SWCNTs in 25 ml

solution. The APTES functionalization procedure starts with the immersion of the substrate in sulphochromic acid for 2.5 minutes. Then the substrate was washed in deionized (DI) water thoroughly to generate OH bonds and dried using N_2 gas. The substrate was heated for 1 hour at 120^oC and a 10^{-2}mbar pressure. A solution of 600 microlitres of 3-aminoisopropyltriethoxysilane and 20ml of isopropyl alcohol (IPA) were made ready for immersion of the substrate. The substrate was immersed for 15 minutes in the prepared solution in argonambient. The argon gas was filled in the chamber to avoid polymerization of APTES.Subsequently, the substrate was rinsed in IPA, dried using argon gas and then kept in a 95% semiconducting purity SWCNTs solution for 70 minutes to deposit SWCNTs. Sodium dodecyl sulphate (SDS) residuals on the SWCNTs were eliminated by dipping the substrate in IPA, then washing in DI water and dried by blown of nitrogen gas. The patterning of SWCNTs was done by O_2 plasma etching to retain SWCNTs only in the channel region. The patterned SWCNTs after O_2 plasma etching is shown in figure 1(e).

The source and drain electrodes of metal palladium/gold (Pd/Au) of thickness 8/20nm was deposited by 4-TEBE and patterned using standard photolithography and lift-off is shown in figure 1(f). The deposition of bigger source, drain, and gate electrode contact pads of metal Ti/Au of thickness 8/50nm was done by RF sputtering and patterned using standard photolithography are shown in figure 1(g).

The CNTTFTs fabricated were of channel length (L) 3, 4, 5, 8, 10,15,20,30,40,50,75 and 100µm and channel width (W) 3,5,8,10,15,20,30,40 and 50µm. As a final step of the fabrication process, the flexible polyimide substrate was removed from the 2 inch silicon wafer.

3.Results and discussion

In this section the discussion on the images of SWCNTs deposited taken by field emission scanning electron microscope (FESEM) and the Raman spectroscopy data of different semiconducting purity SWCNTs on gate dielectrics, electrical characterization comparison and the study of extractedelectrical parameters the normalized on current (I_{ON}/W), on-off current ratio (I_{ON}/I_{OFF}), transconductance (g_m) and carrier mobility ($\mu_{carr.}$) of flexible CNTTFTs which uses 95% semiconducting purity SWCNTs (95CNTTFTs) and 99.99% semiconducting purity SWCNTs (99CNTTFTs) with varying channel length (L) and width (W).

3.1 Images and Raman spectroscopy data of SWCNTs thin film, and photographs of fabricated CNTTFTs

To know the density of the deposited SWCNTs on the polyimide substrate the FESEM image was taken is displayed in figures 2(a) and 2(c) respectively. In both the cases, the density of the SWCNTs deposited is around 105nanotubes/µm^2. The Raman spectroscopy data was used to evaluate the semiconducting purity of the SWCNTs and to find whether the presence of metallic nanotubes is lower or higher. The Raman spectroscopy radial breathing modes (RBM) data of the deposited 95% semiconducting purity SWCNTs shows peaks after 200cm^{-1} which specifies the existence of some percentage of metallic carbon nanotubes[26] are as seen in figure 2(b). But the Raman spectroscopy RBM data deposited of 99.99% semkiconducting purity SWCNTs shows the spectroscopic peaks concentrated less than 200cm^{-1} specifies the presence of almost no metallic carbon nanotubes and higher semiconducting nanotubes[26] are as seen in figure 2(d). Figure 3(a) and 3(b) shows the images of SWCNTs made contact with one of the Pd electrodes.

Photograph of the polyimide substrate on which the CNTTFTs were fabricated after it was removed from the 2 inch Si substrate is as seen in figure 4(a). Microscopic images of an array of 4 flexible CNTTFTs fabricated on the polyimide substrate are shown in figure 4(b). Microscopic image of a CNTTFT of L=4µm, W=30µm is as seen in figure 4(c). The FESEM image of CNTTFTs fabricated were taken and shown in figure 4(d).

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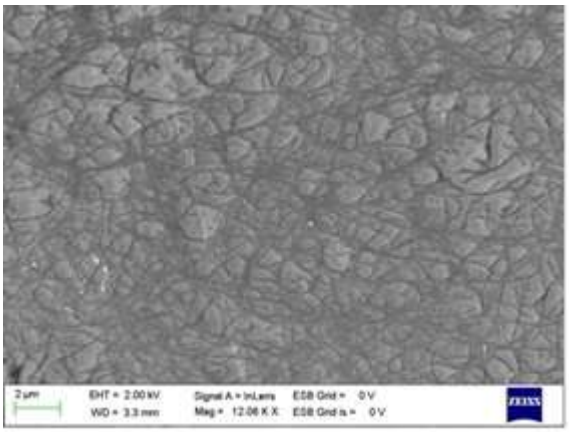
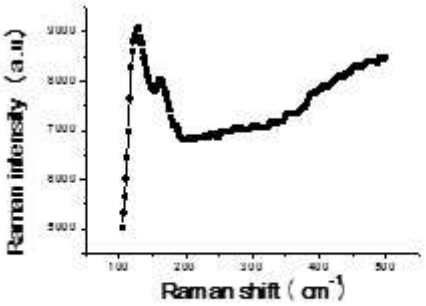


(a)



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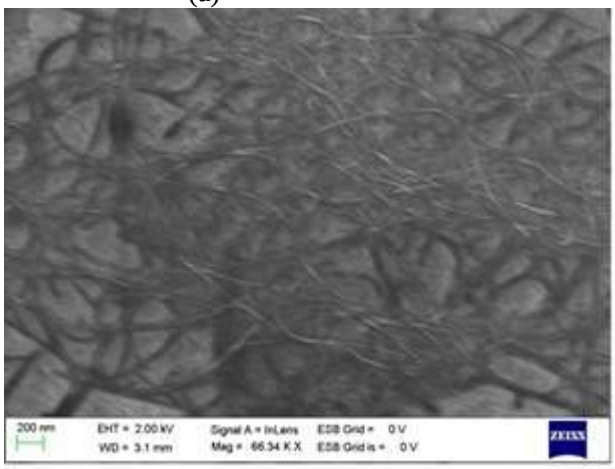

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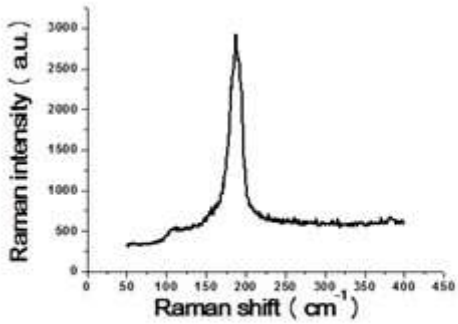
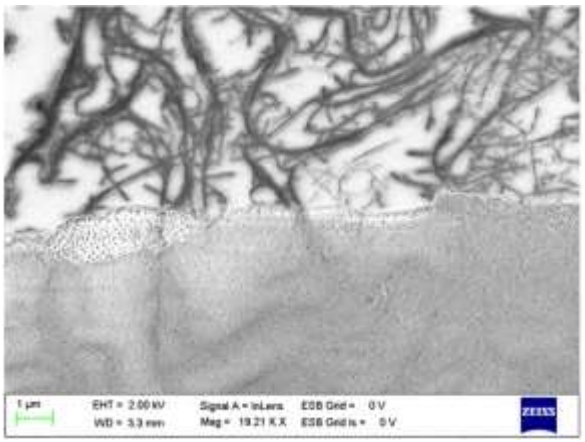
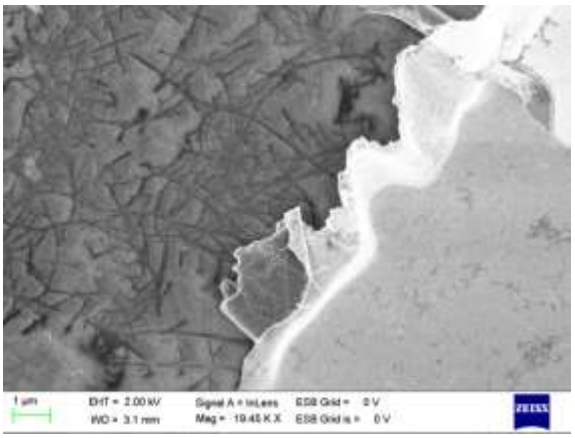


(d)

Figure 2. FESEM images and Raman spectroscopy data of SWCNTs. (a) FESEM image of 95% purity SWCNTs deposited. (b) Raman spectroscopy data of deposited SWCNTs of 95% purity. (c) FESEM image of 99.99% purity SWCNTs deposited. (d) Raman spectroscopy data of deposited SWCNTs of 99.99% purity.



(a)



(b)

Figure 3. FESEM images of SWCNTs made contact with electrodes. (a), (b) SWCNTs established contact with one of the Pd electrodes.

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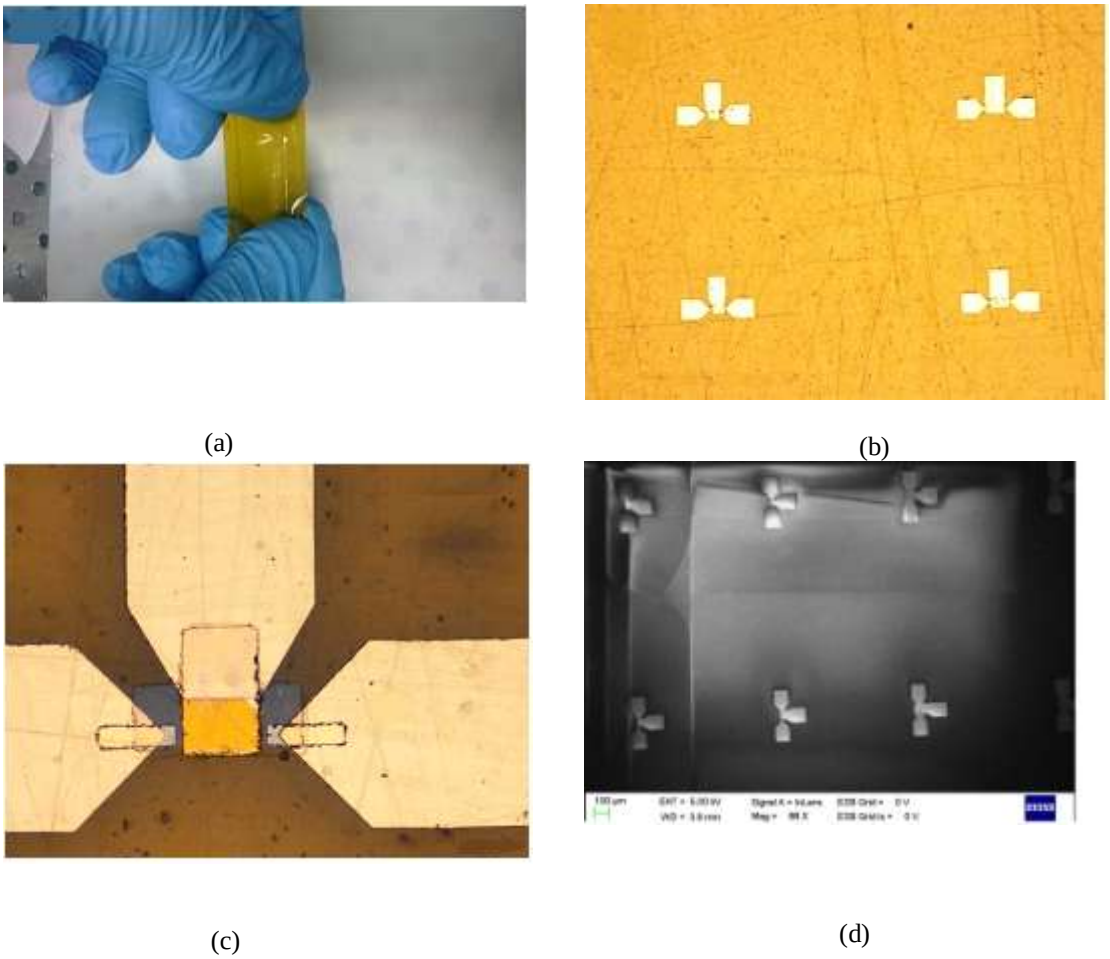

Figure 4. Microscopic images, photograph, and FESEM image of the fabricated flexible CNTTFTs. (a) Photograph of the polyimide substrate removed from the Si wafer. (b) Microscopic images of the 4 CNTTFTs fabricated on a polyimide substrate. (c) Microscopic image of a CNTTFT of L= 4 µm, W= 30 µm. (d) FESEM image of fabricated flexible CNTTFTs

3.2 Electrical characterization

Electrical characterization of the CNTTFTs which uses 95% and 99.99% semiconducting purity SWCNTs was conducted. The electrical characterization of flexible CNTTFTs was done using fast IV-measurement Agilent B 1500A semiconductor device analyzer. The electrical performance parameters on current, on-off current ratio, transconductance, the mobility of 95CNTTFTs and 99CNTTFTs are calculated and plotted against the channel length with varying widths for the comparison. The output characteristics of 95CNTTFT and 99CNTTFT of L=50µm, W=50µm are as seen in figures 5(a) and (b) respectively. The output characteristics of 95CNTTFT and 99CNTTFT exhibited p-type behavior. The peak on saturation current measured at V_{GS}=-25V for 95CNTTFT and 99CNTTFT are 992.56 µA and 812.59µA respectively. The peak saturation current in 95CNTTFT observed is more when compared to the 99CNTTFT because of the presence of more metallic nanotubes in the 95% semiconducting purity SWCNTs compared to the 99.99% semiconducting purity SWCNTs. The extracted output drain conductance of the 95CNTTFT and 99CNTTFT at V_{GS} =-15 V are 29.78 µS and 26.37 µS respectively. The transfer characteristics of both 95CNTTFT and 99CNTTFT at V_{DS}= -40V is shown in figure 5(c). The measured on drain currents of 95CNTTFT and 99CNTTFT are almost same at the higher magnitude of V_{GS}, because at higher magnitudes of V_{GS} the semiconducting nanotubes are also started conducting as metallic

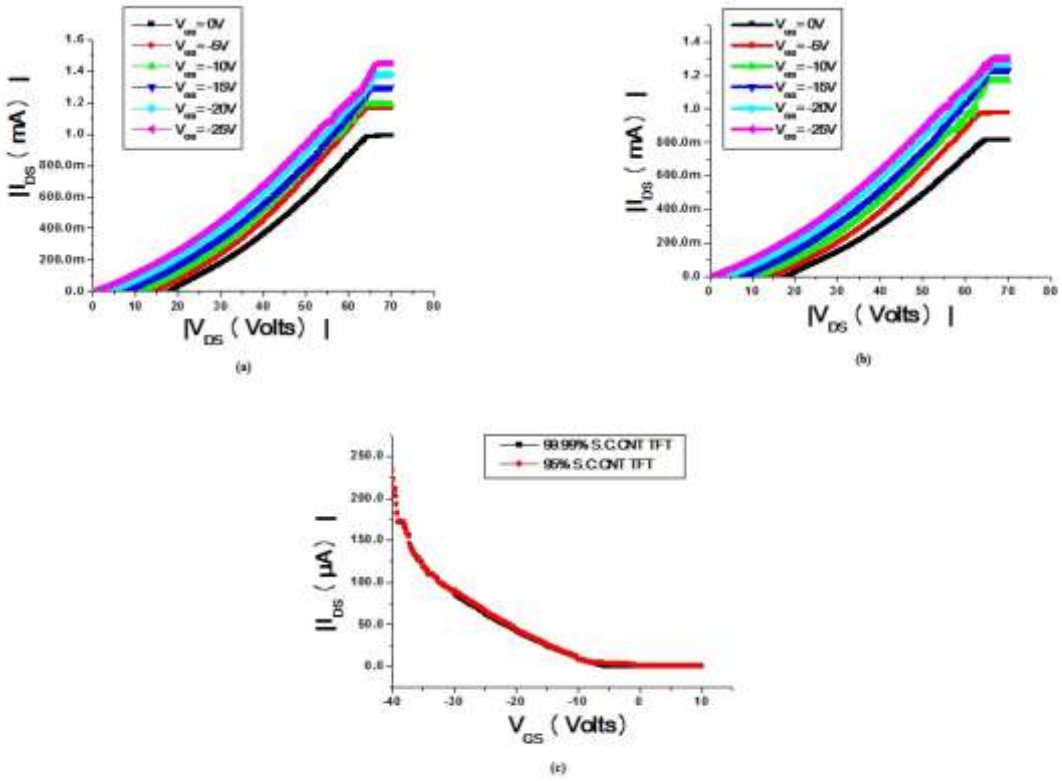

Figure 5. I-V characteristics of flexible bottom-gate CNTTFTs. (a) Output characteristics of the CNTTFT which used 95% semiconducting purity SWCNTs for the channel thin film. (b) Output characteristics of the CNTTFT which used 99.99% semiconducting purity SWCNTs for the channel thin film formation. (c) Transfer characteristics of the CNTTFTs at a drain to source voltage (V_{DS}) of -40 V which used 95% and 99.99% semiconducting purity SWCNTs.

nanotubes [27] whereas the higher current is measured at lower values of V_{GS} for 95CNTTFT than 99CNTTFT because of the existence of more metallic nanotubes in the SWCNTs present in the channel area of 95CNTTFT compared to 99CNTTFT.

3.2.1 Electrical characteristics parameters extraction and plots

The extracted electrical characteristics parameters on current (I_{ON}), normalized on current or on current density, on-off current ratio, transconductance, carrier mobility are estimated and plotted against channel length is shown in the figure 6 .

Using the equation (1) carrier mobility is calculated.

$$\mu_{carr.} = Lg_m / V_{DS} C_{ox} W \quad (1)$$

Where L and W are the channel length and width of flexible CNTTFT, V_{DS} =drain to source voltage, C_{ox} is the gate capacitance per unit area. The C_{ox} is estimated using equation (2) and is estimated by taking into consideration the electrostatic coupling between the nanotubes [28, 29, 30].

$$C_{ox} = \{C_Q^{-1} + (1/2\pi\varepsilon_o\varepsilon_{ox}) \ln[(\Lambda_o \sinh(2\pi t_{ox}/\Lambda_o))/R\pi]\}^{-1} \Lambda_o^{-1} \quad (2)$$

1/ Λ_o be regarded as the nanotubes linear density and is about 10 tubes/µm, the value of nanotubes quantum capacitance C_Q considered from the work [31] is 4 X10-12 F/cm, t_{ox} is the oxide thickness = 40 nm, the value of the radius of nanotubes R =1.5nm and the dielectric constant ($\varepsilon_0\varepsilon_{ox}$) at the interface where the nanotubes are placed is 3.9 X 8.85X10-14 F/cm. The value of C_{ox} estimated using equation (2) is 4.0091X10-8 F/cm2. The estimated values of C_{ox} and g_m are used in the equation (1) to calculate $\mu_{carr.}$ of

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95CNTTFT and 99CNTTFT of L=50µm,W=50µm. The estimated values of $\mu_{carr.}$ of 95CNTTFT and 99CNTTFT are 4.68 cm^2/Vs and 4.61 cm^2/Vs respectively.

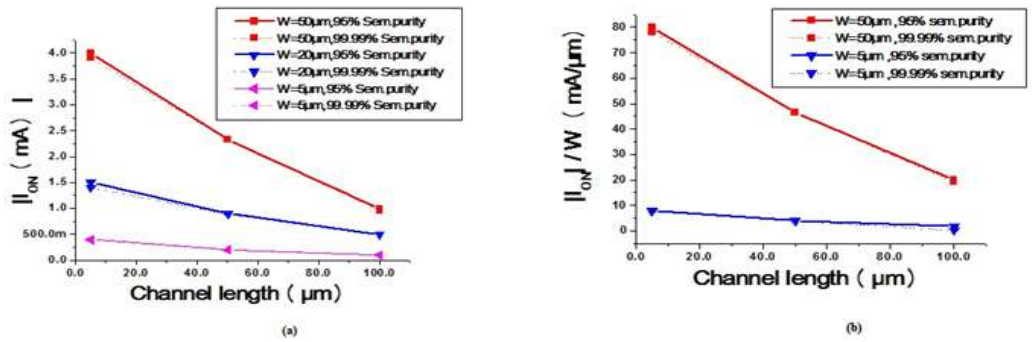
The on-current plotted against channel length is as seen in figure 6(a). The measured on-current of the 95CNTTFT of L=5µm,W=50µm is 4mA. It indicates that the on current is highest for devices of shorter channel length and higher width. With the increase in channel length and the decrease of a channel width of both 95CNTTFT and 99CNTTFT the on-current decreases. The on-current of 95CNTTFT is little more when compared to the 99CNTTFT for the identical dimensions of devices. The increase of current as the width increases is due to the more number of carbon nanotubes are participating in carrying the current. The on-current density (I_{ON}/W) plotted against channel length for 2 different widths of 5µm and 50 µm is as seen in figure 6(b).

The on current density also reduces with the increase of length and the decrease of a width of 95CNTTFT and 99CNTTFT. The measured maximum on current density of 95CNTTFT and 99CNTTFT of L=5µm,W=50µm are 0.08 mA/µm and 0.078 mA/µm respectively. The on-off current ratio variation with channel length is as seen in figure 6(c).

The on-off current ratio increases with the increase of channel length in both 95CNTTFTs and 99CNTTFTs. This is due to the possible bridging of metallic carbon nanotubes between the source and drains in short channel length devices than long channel length devices of both the types. The 95CNTTFT on-off current ratio is lower than the 99CNTTFTs for a particular dimension of the device. This is because of the current when the device is off is more in the 95CNTTFTs than 99CNTTFTs due to the existence of more number of metallic SWCNTs in 95CNTTFTs. The metallic SWCNTs conduct at very lower and with no gate potentials also. Because the carbon nanotube network comprises of semiconducting and metallic nanotubes, if the density of metallicnanotubes crosses the percolation threshold then the network will become metallic. In order to attain the highest current drive with good off-state characteristics, the fraction of metallic nanotubes will have to be reduced [32]. The maximum on-off current ratio exhibited by 99CNTTFT of L=5µm, W=50µm is $1.49X10^4$. For the same dimensions, the maximum on-off current ratio shown by 95CNTTFT is $2.307X10^3$. These values are higher than the on-off current ratio reported in [33].

As the channel length increases the transconductance (g_m) of both the types of CNTTFTs decreases is as shown in figure 6(d). The variation of transconductance is inversely related to the channel length of the devices. As the channel length increases the channel resistance increases and it effects the transconductance adversely[3]. The highest normalized trans conductance (g_m/W) of 99CNTTFT and 95CNTTFT of L=5µm, W=50µm exhibited in the present work are 3.164µS/µm and 2.44µS/µm respectively. These values are higher than the value of g_m/W = 0.1 µS/µm reported in [3]. The observed values of on-off ratio and transconductance are high in the this work because of the higher density of deposited SWCNTs. The carrier mobility increases with the increase in channel length of both the types of devices 95CNTTFT and 99CNTTFT is due to the electron scattering dominated at the metal-nanotube contacts than the electron scattering in the channel [3] is shown in figure 6(e). The similar variation is observed in the CNTTTFTs of the work [34,35]. The highest carrier mobility observed in the present work is 5.55 Cm^2/Vs for the 99CNTTFT of L=100 µm, W=50 µm and for 95CNTTFT of same dimensions exhibits 5.03 Cm^2/Vs. The higher carrier mobility is exhibited in this work is than CNTTFTs in [33] because of the higher semiconducting purity and density of the SWCNTs deposited than the CNTTFTs in [33].

Subthreshold swing exhibited by 99CNTTFT and 95CNTTFT of L=W=50µm of this work are 716.94mV/decade and 933 mV/decade respectively. The subthreshold swing reported in [36] is 1200 mV/decade for a device L=W=100µm. The subthreshold swing of the present work is lower than the CNTTFTs in [36] since the deposition density of SWCNTs is higher and the gate dielectric used is of higher dielectric constant compared to the used in [36].



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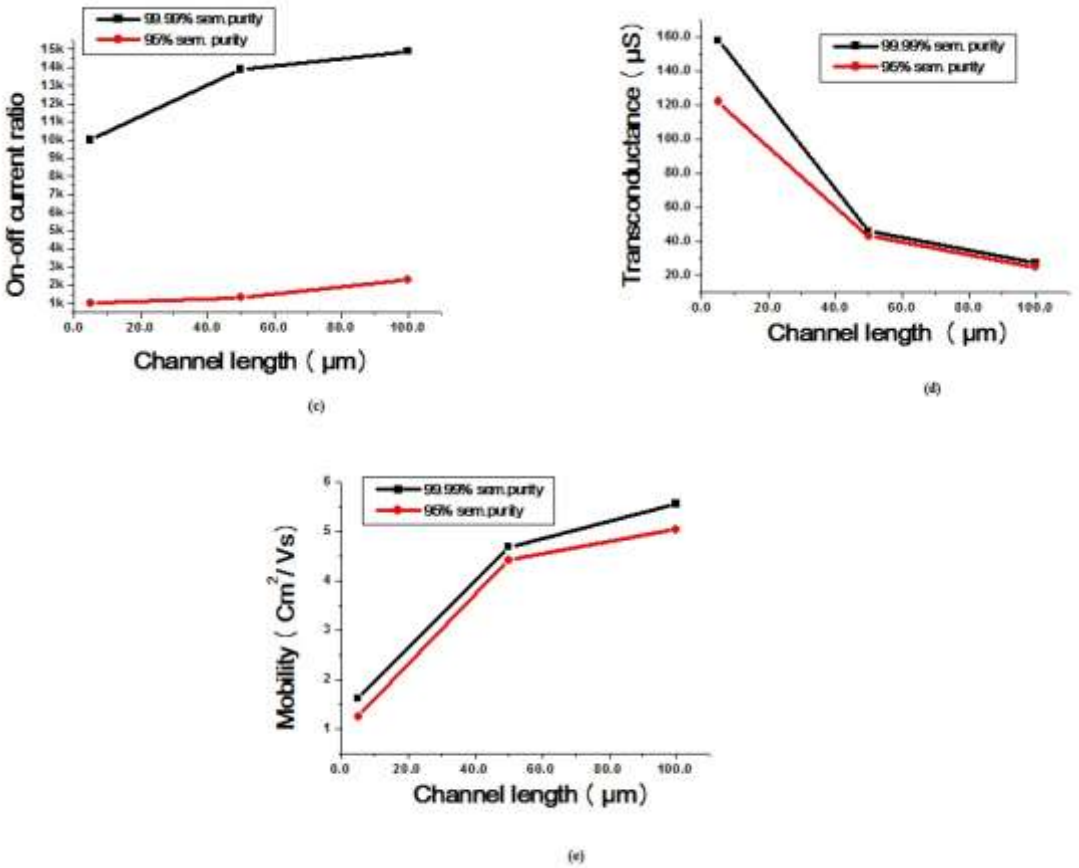

Figure 6.Electrical performance parameters variation against channel length of 95CNTTFTs and 99CNTTFTs. (a) On current variation against channel length with various W. (b) On-off current ratio variation against channel length (with W=50 µm). (c) Current density against channel length with various values of W. (d) Trans conductance variation against channel length (with W=50 µm). (e) Mobility variation against channel length (with W=50 µm).

4. Conclusion

In this work, the fabrication of bottom-gate flexible CNTTFTs using 99.99% and 95% semiconducting purity SWCNTs and the effect of semiconducting purity of SWCNTs on the electrical performance of the flexible CNTTFTs was demonstrated. In both flexible CNTTFTs the deposition density of the SWCNTs was higher around 105 CNTs/µm^2. In both the cases, the extracted electrical performance parameters I_{ON}, I_{ON}/W and gm decrease with the increase in channel length of the flexible CNTTFTs, whereas the I_{ON}/I_{OFF} and µcarr. increases. The flexible CNTTFTs with 99.99% semiconducting purity SWCNTs have outperformed the flexible CNTTFTs with 95% semiconducting purity SWCNTs in on-off current ratio, transconductance, mobility, subthreshold swing because higher semiconducting purity SWCNTs were used. The flexible CNTTFTs of present work have demonstrated higher I_{ON}/I_{OFF}, gm and µcarr. compared with the CNTTFTs considered from the literature because high dielectric constant HfO_2 was used as gate dielectric and higher deposited semiconducting purity and density of the SWCNTs. This work demonstrates that for the better electrical performance of flexible CNTTFTs should have SWCNTs of higher semiconducting purity and density.

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References

[1]. Ishikawa F N, Chang H-K, Ryu K, Chen P-C, Badmaev A, Gomez L, Arco D, Shen G and Zhou C, "Transparent electronics based on transfer printed aligned carbon nanotubes on rigid and flexible substrates," ACS Nano,Vol. 3, pp.73–9,2009.

[2]. Sun D-M., Timmermans M Y, Tian Y., Nasibulin A. G., kauppinen E., Kishimoto S., Mizutani T and OhmoY, "Flexible high-performance carbon nanotube integrated circuits," Nat. Nanotechnol.,Vol.6, pp.156–61, 2011.

[3]. Chandra B., Park H. S., Maarouf A., Martyna G. J. andTulevski G. S., "Carbon nanotube thin film transistors on flexible substrates,"Appl.Phys. Lett., Vol.99, pp. 072110, 2011.

[4]. Wang C, Chien J-C, Takei K, Takahashi T, Nah J, Ali M. Niknejad, and Javey A, "Extremely bendable, high-performance integrated circuits using semiconducting carbon nanotube networks for digital, analog, and radio-frequency applications," Nano Letters,Vol.12, pp. 1527-33, 2012.

[5]. Takahashi T., Takei K., Gillies A. G., Ronald S. Fearing and Javey A., " Carbon nanotube active-matrix backplanes for conformal electronics and sensors," Nano Letters, Vol.11, pp. 5408-13, 2011.

[6]. Gao P. and Qing Z., "Encapsulate-and-peel: fabricating carbon nanotube CMOS integrated circuits in a flexible ultra- thin plastic film," Nanotechnology,Vol.25, pp.065301-7, 2014.

[7]. Cao Q, Kim H, Pimparkar N, Kulkarni J P, Wang C, Shim M, Roy K, AlamMA and Rogers J A., " Medium- scale carbon nanotube thin film integrated circuits on flexible plastic substrates,"Nature,Vol.454 , pp.495–500, 2008.

[8]. Chandrashekhar M. C. and Narasimhamurthy K.C, "Fabrication,electrical characterization and mechanical flexibility test of back gated carbon nanotube thin film transistorson polyimide substrate," Materials Research Express, Vol.5, pp.126304-10,2018.

[9]. Jang S., Jang H., Lee Y., Suh D., Baik S., Hong B. H. and Ahn J. H.,"Flexible, transparent single-walled carbon nanotube transistors with graphene electrodes," Nanotechnology, Vol.21, 425201-4, 2010.

[10].Cao X, Chen H, Gu X, Liu B, Wang W, Cao Y, Wu F and Zhou C,"Screen printing as a scalable and low-cost approach for rigid and flexible thin-film transistors using separated carbon nanotubes,"ACS Nano,Vol.8, pp.12769–76, 2014.

[11].Ishikawa F N, Chang H-K, Ryu K, Chen P-C, Badmaev A, Gomez L, Arco D, ShenG and Zhou C,"Transparent electronics based on transfer printed aligned carbon nanotubes on rigid and flexible substrates,"ACS Nano,Vol.3,pp.73–9, 2009.

[12].Forrest S. R., "The path to ubiquitous and low-cost organic electronic appliances on plastic. Nature,Vol.428, pp.911–8, 2004.

[13].Dimitrakopoulos C. D., and Masaccro D. J., "Organic- thin film transistors: a review of recent advances," IBMJ Res. Dev., Vol.45, pp.11, 2001.

[14].Street R. A. , "Technology and Applications of Amorphous Silicon,"(Berlin: Springer),2000.

[15].Kumar S., Baratunde A. Cola, Jackson R., & Graham S. " A Review of carbon nanotube ensembles as flexible electronics and advanced packaging materials," Journal of Electronic Packaging,Vol.133, pp.020906-12, 2011.

[16].Narasimhamurthy K C & Paily R.,"High-performance local back gate thin-film field–effect transistors using sorted carbonnanotubes on an amino-silane treated hafnium oxide surface," Semicond. Sci. Technol., Vol.26, pp. 07500, 2011.

[17].Tian B, Liang X, Yan Q, Zhang H, Xia J, Dong G, Peng L and Xie"Wafer scale fabrication of carbon nanotube thin film transistors with high yield," J. Appl. Phys., Vol.120, pp. 034501, 2016.

[18].Paul L. M. E. &Ji-Yong P., "Electron transport in single-walled carbon nanotubes,"MRS Bulletin,Vol.29,pp.272-5, 2004.

[19].Tsuneya A. and Takeshi N., "Impurity scattering in carbon nanotubes – Absence of Back Scattering ," J. Phys. Soc J., Vol.67, pp.1704-1713,1998.

[20].Paul L. M. E., Marc B., David H., Cobden, Young-G .Y., and Steven G. L., "Disorder, pseudospins, and backscattering in carbon nanotubes,"Phys. Rev. Lett., Vol.83, pp. 5098, 1999.

[21].Hiromichi Kataura, "Theory of electronic states and transport in carbon nanotubes," JPSJ,Vol. 2, pp.777-84, 2005.

[22].Eizo Otsuka, "Electron scattering by impurities in semiconductors," Jap. J. Appl. Phy., Vol. 25, pp.303, 1985.

[23].Min O., JIN-L. H. and Charles M. L.,"Fundamental electronicproperties and applications of single-walled carbon nanotubes,"Acc. Chem. Res.,Vol.35,pp.1018-25, 2002.

[24].Chandrashekhar M. C. and Narasimhamurthy K.C, "Comparison of electrical performance and stability of flexible carbon nanotube thin film transistors of different gate strucures," International Journal of Electronics Engineering,Vol.10, No.2, pp.673-680, 2018

[25].LeMieux M. C., Roberts M., Barman S., Jin Y. W., Kim J. M. and Bao Z., "Self –sorted, aligned nanotube networks for thin-film transistors," Science,Vol.321, pp. 101–4, 2008.

[26].H Kataura, Kumazawa, Y.Maniwa, I Umezu, S Suzuki,Y Ohtsuka, and Y achiba,"Optical properties of single-wall carbon nanotubes," Synth. Met. Vol.103 (1-3), pp.2555-2558, 1999.

[27].Narasimhamurthy K. C. and Paily R., "Performance comparison of thin-film transistors fabricated using different purity semiconducting nanotubes," 24th International Conference on VLSI Design , 2011.

[28].Kang S. J., Kocabas C., Ozel T., Shim M., Pimparkar N., Alam M. A and Rogers J. A., "High- performance electronics using dense, perfectly aligned arrays of single- walled carbon nanotubes," Nat. Nanotechnol. Vol.2, pp.230–6, 2007.

[29].Cao Q., Xia M., Kocabas C., Rogers J. A. and Rotkin S. V., "Gate capacitance coupling of single- walled carbon nanotube thin- film transistors. Appl. Phys. Lett., Vol. 90, pp.023516, 2007.

[30].Wang C., Zhang J. and Zhou C., "Macro electronic integrated circuits using high- performance separated carbon nanotube thin film transistors," ACS Nano,Vol. 4, pp.7123–32, 2010.

[31].Rosenblatt S., Yaish Y., Park J.,Gore,Sazonova V. and McEuen P. L., "High performance electrolyte gated carbon nanotube transistors," Nano Lett., Vol. 2, pp.869-72, 2002.

[32].Snow E. S., Novak J. P., Campbell P. M. and Park D., "Random networks of carbon nanotubes as an electronic material,"Applied Physics Letter,Vol.82, pp. 2145-7, 2003.

[33].Jang S., Jang H., Lee Y., Suh D., Baik S., Hong B. H. and Ahn J., "Flexible, transparent single-walled carbon nanotube transistors with graphene electrodes. Nanotechnology, Vol.21,pp.425201–6, 2010.

[34].Narasimhamurthy K. C. and Paily R., Performance comparison of interdigitated thin-film-field effect transistors using different purity semiconducting carbon nanotubes. Advanced materials research ,Vol.181-2, pp.343-348, 2011.

[35].Ko H.and Tsukruk V. V.,"Liquid-crystalline processing of highly oriented carbon nanotube arrays for thin-film transistors," Nano Lett., Vol.6, pp.1443–8, 2006.

[36].Zhang J., Wang C. and Zhou C., "Rigid/flexible transparent electronics based on separated carbon nanotube thin film transistors and their application in display electronics," ACS nano,Vol.6,pp.7412-19, 2012.