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Design & Implementation of 16-bit Parity Preserving Ripple Carry Adder

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Abstract: Adders are the main building blocks of digital circuits to perform all the arithmetic operations. Parity preserving adders are very important to identify the errors in the digital system. In this paper, proposed designs of 16-bit parity preserving ripple carry adder are presented. This parity preserving adder makes use of reversible logic LCG and ZPLG gates. The proposed modified adder is more efficient in terms of quantum cost and garbage outputs. Therefore, this reversible logic design has applications in low power CMOS and nanotechnology.
Keywords: Reversible logic, parity preserving LCG, ZPLG, Ripple Carry Adder.

1. Introduction

Reversible computation overcomes the problems that occur in irreversible computation. Therefore, reversible computation is getting attention in various fields. In 1961, R.Landauer [1] described that loss of each information bit is associated with the heat dissipation of KTLn2, where k is Boltzmann's constant and T is the temperature of the system. In 1973, C.H. Bennett described that this heat dissipation problem can be solved by using reversible logic gates in the circuit [2].

In reversible logic gates, input can be retrieved from the output [3]. There is one to one mapping between inputs and outputs of the circuit.

Some important factors for reversible logic gates are:

i) Constant Input: Inputs which are maintained constant either at 0 or 1 are known as constant input.

ii) Quantum cost: Cost of the circuits in term of primitive gates (1*1 or 2*2) is known as quantum cost. Quantum cost can be realized by counting the number of CNOT and Controlled-V logic in the circuit [4].

iii) Garbage outputs: Garbage outputs are the unwanted outputs that are necessary to maintain the reversibility of the circuit.

2. Some Reversible Logic Gates:

2.1. FEYNMAN GATE: Feynman gate is a 2*2 reversible gate. Quantum cost of Feynman gate is 1. Fig. 1 represents the block diagram of Feynman gate.

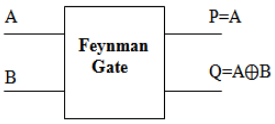

Figure 1. Block diagram of Feynman gate

2.2. LCG GATE: Low Complexity Gate (LCG) is a 5*5 gate. Quantum cost of this gate is 10. Fig. 2 represents the block diagram of LCG gate.

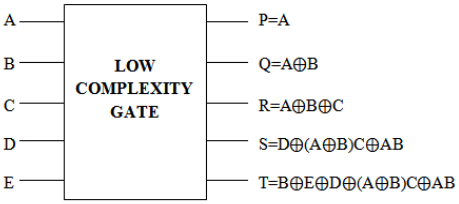

Figure 2. Block diagram of LCG gate

2.3. TOFFOLI GATE: Toffoli gate is a 3*3 reversible gate. Quantum cost of Toffoli gate is 5. Fig. 3 represents the block diagram of Toffoli gate.

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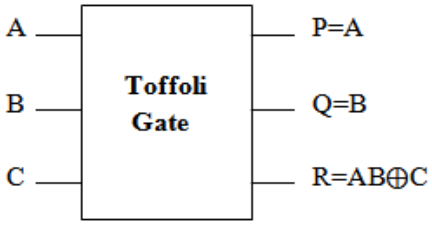

Figure 3. Block diagram of Toffoli gate

2.4. ZPLG GATE: ZPLG is also a 5*5 gate. Quantum cost of this gate is 8. Fig. 4 represents the block diagram of ZPLG gate.

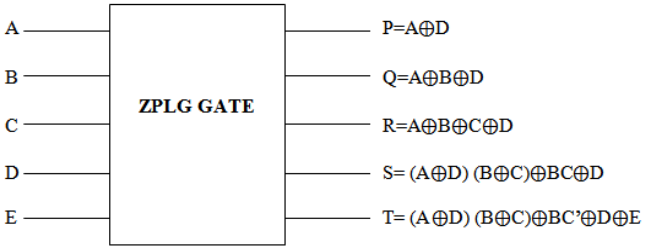

Figure 4. Block diagram of ZPLG gate

3. Literature Survey

In 2012, B. Raghu Kanth et al. depicted the comparison between reversible and conventional logic gates. Reversible DKG gate was used to perform addition/subtraction and then the performance was compared with conventional gates. The result was better for reversible adder circuit than conventional gates in terms of power consumption, delay and garbage outputs [5].

In 2014, Nidhi et al. described an efficient design of ripple carry adder and carry skip adder using 4*4 MSTG gate, 4*4 MHNG gate and 3*3 MFRG gate. These proposed designs were superior to the existing designs in terms of hardware complexity and quantum cost [6].

In 2015, Manoj kumar et al. depicted that the design of ripple carry adder, carry save adder, carry skip adder and carry bypass adder using reversible logic gates assures zero heat dissipation [7].

In 2016, Gowthami P et al. presented the design of ripple carry adder circuits using PFAG and HNG reversible gates. Delays of these circuits were less as compared to conventional ripple carry adder [8].

In 2016, Ankush et al. proposed a design of low power reversible carry skip adder using modified HNG and modified FRG gates. Quantum cost and power consumption of carry skip adder was optimized by using these reversible gates [9].

In 2018, K Arunamanjusha et al. described the comparison between conventional ripple carry adder and reversible ripple carry adder. Reversible RCA using reversible Peres and HNG offered less quantum cost and required less number of gates as compared to conventional adder [10].

4. Proposed work:

4.1 1st Proposed 16-bit Ripple Carry Adder using LCG gate

In ripple carry adder, each carry gets rippled into the next stage. First element needed to design a ripple carry adder is a full adder. 16-bit RCA can be constructed using 16 LCGs as represented below in Fig.5. LCG gate used to construct a RCA is a parity preserving gate. LCG gate operates as a full adder if two last inputs (D and E) of LCG are set to zero [11]. Quantum cost of one LCG gate is 10.

Quantum cost of RCA=n*(quantum cost of one LCG)

where, n is the number of LCGs used to construct RCA. Total quantum cost of 16-bit RCA using LCGs is 160.

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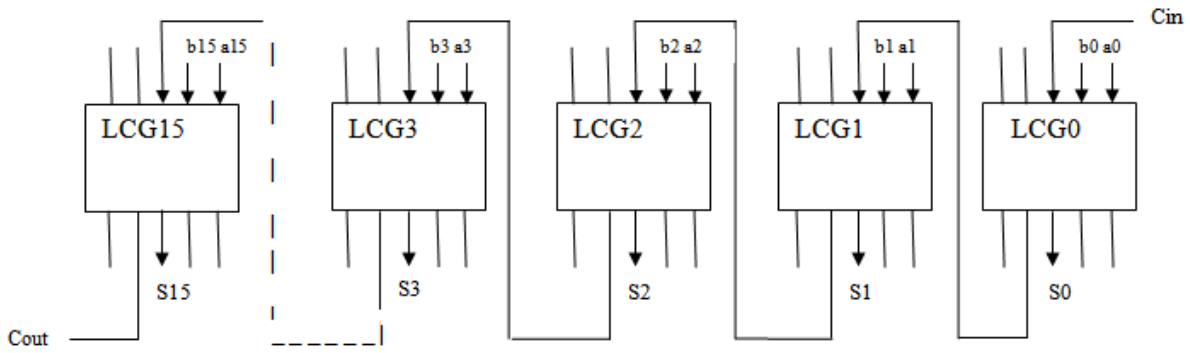
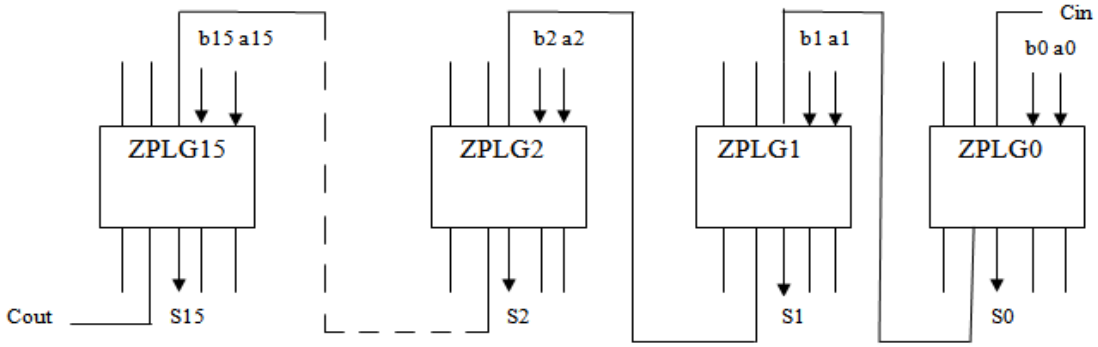


Figure 5. 16-bit RCA using LCG gates

4.2 2nd Proposed Modified Ripple Carry Adder using ZPLG gate

RCA can also be constructed by using ZPLG gate instead of LCG gate. ZPLG gate operates as a parity preserving gate by maintaining last two inputs (D and E) at constant zero. Quantum cost of ZPLG gate is 8 which is less as compared to LCG gate [11].



Total quantum cost of modified-16-bit RCA using ZPLGs is 128 and this design is represented in Fig.6.

Figure 6. 16-bit RCA using ZPLG gates

4. Implementation and Results

Table 1. Comparison of 1st Proposed and 2nd Proposed modified 16-bit RCA

16-bit RCA	Power Consumption (W)	Quantum cost
1st Proposed 16-bit design using LCGs	2.827	160
2nd Proposed Modified 16-bit design using ZPLGs	1.445	128

5. Simulation Methodology

5.1 Simulation Methodology for RCA using LCG

Xilinx ISE 14.4 and VHDL code is used to simulate 16-bit RCA. Fig. 7 shows the RTL view of proposed 16-bit RCA using LCG gates. It contains inputs a, b each of which contains 16 bits and Cin as the input carry. It has output S which contains 16 bits and Cout as the output carry.

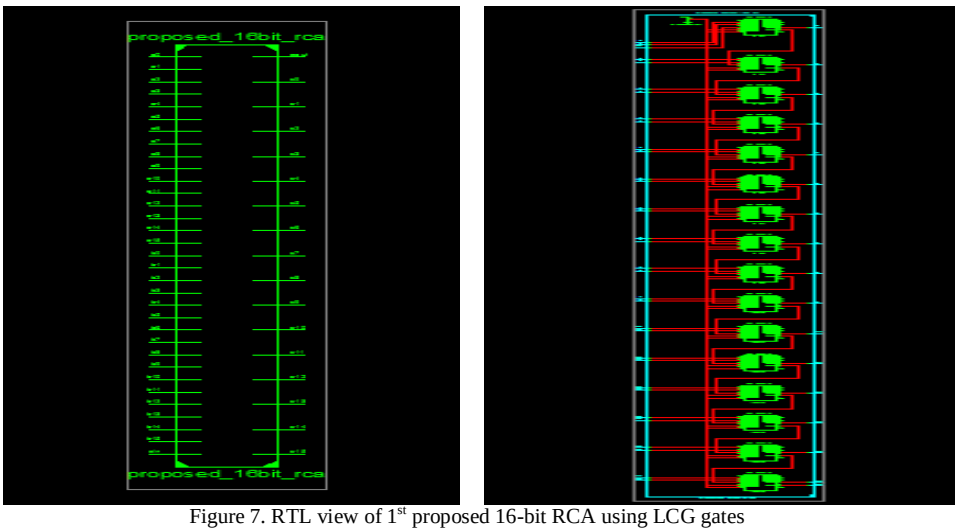


Figure 7. RTL view of 1st proposed 16-bit RCA using LCG gates

5.2 Simulation Methodology for RCA using ZPLG gate

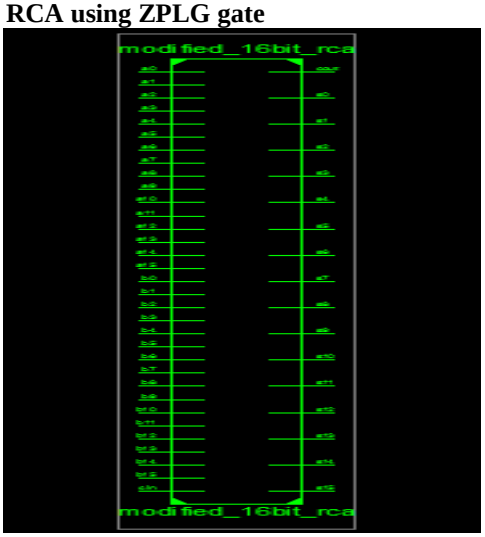


Fig. 8 shows the RTL view of proposed modified 16-bit RCA using ZPLG gates. It also contains inputs a, b each of which contains 16 bits and Cin as the input carry. It has output S which contains 16 bits and Cout as the output carry.

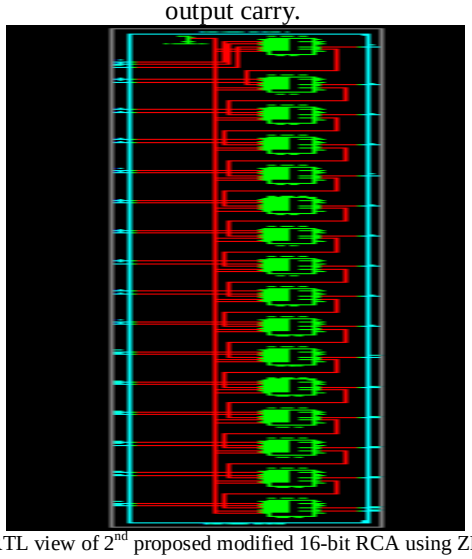


Figure 8. RTL view of 2nd proposed modified 16-bit RCA using ZPLG gates

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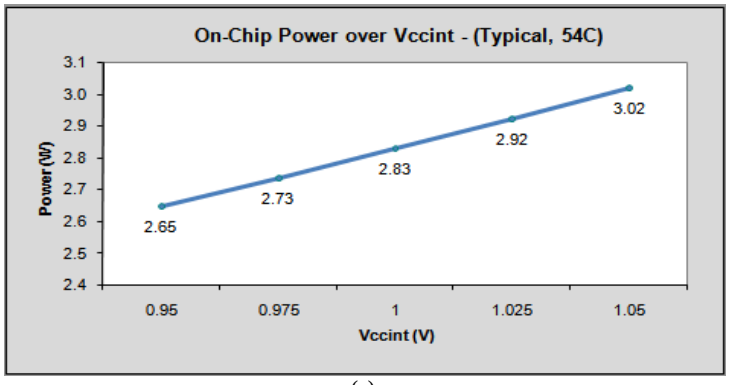
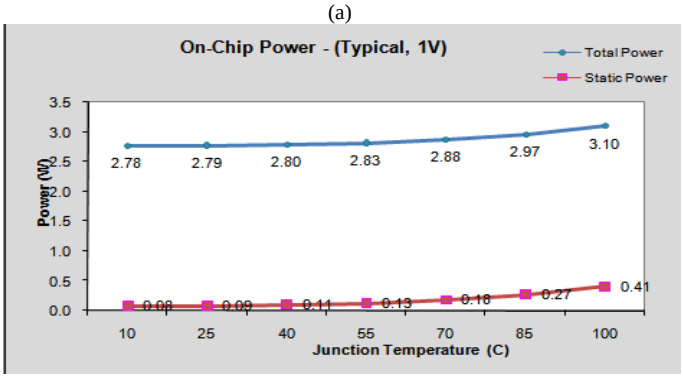
5.3 Power Results

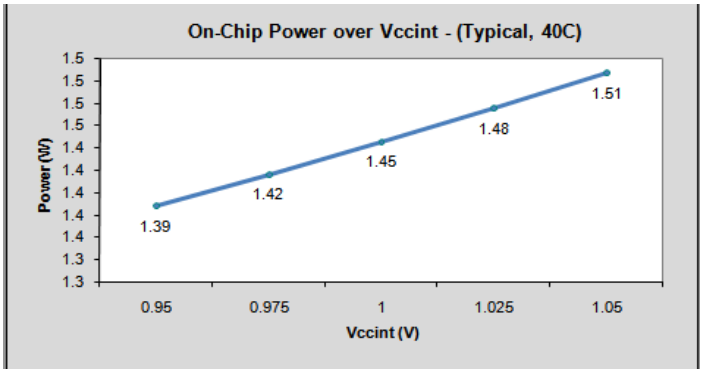


(a)

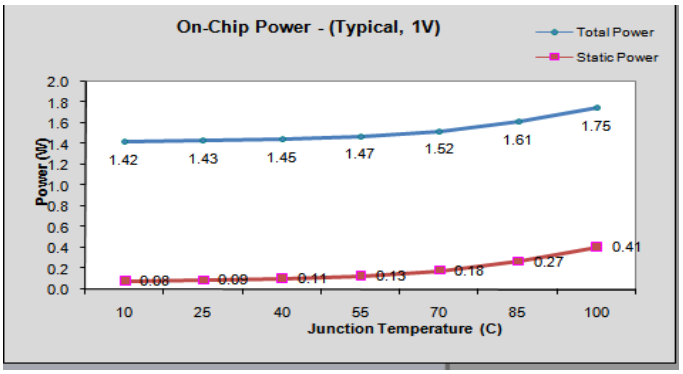


(b)

Figure 9. Graphs (a) and (b) showing power consumption for proposed modified 16-bit Ripple Carry Adder using LCG gates

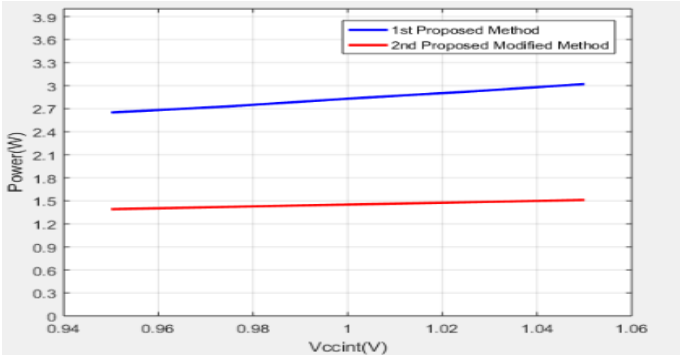


(a)

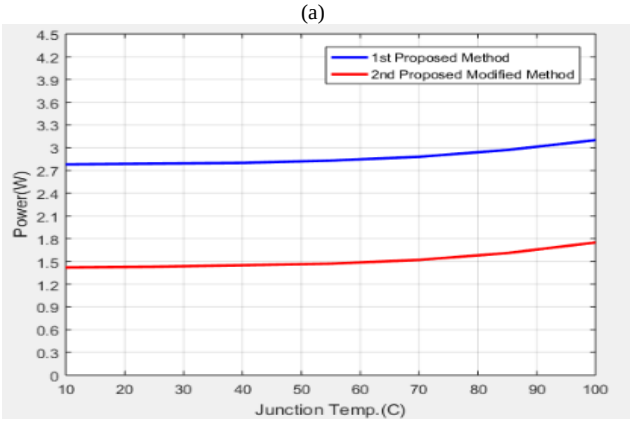


(b)

Figure 10. Graphs (a) and (b) showing power consumption for proposed modified 16-bit Ripple Carry Adder using ZPLG gate



(a)



(b)

Figure 11. (a) and (b) shows Comparative results of Power consumption for proposed RCA using LCG gate and proposed modified RCA using ZPLG gates.

6. Conclusion and Future work

In this paper, 16-bit RCA is presented with the aim of being both low quantum cost and low power consumption. Reversible gates should be chosen carefully for implementing logic function with low quantum cost and low power consumption. For further work, these proposed designs can be extended to n-bit parity preserving adders.

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