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A Low-Power Broad-Bandwidth Noise Cancellation VLSI Circuit Design for In-Ear Headphones

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Abstract: Traditional dynamic clamor crossing out (ANC) earphones regularly perform well in diminishing the low recurrence commotion and confining the high-recurrence clamor by ear covers inactively. The current ANC frameworks regularly utilize fast advanced flag processors to offset irritating commotion, which brings about high power utilization for a business ANC earphone. The commitment of this paper can be grouped into: 1) legitimate channel length choice; 2) low-control stockpiling component for convolution operation; and 3) high-throughput pipelining engineering. With these novel procedures, we build up a range/control effective ANC circuit by utilizing the TSMC 90-nm CMOS innovation for in-ear earphone applications. The proposed sustain forward sifted x slightest mean square ANC circuit configuration gives the highlights of utilizing lower working recurrence and expending significantly less power that encourage preferable execution over the customary ANC earphones.
Index Terms: Active Noise Cancellation, Feedforward Filtered-X Least Mean Square (Fxlms), In-Ear Headphone, VLSI Design.

1. INTRODUCTION

Active noise control technique can attenuate low-frequency noise in ducts, headphones, home window applications, high-speed elevator, and yacht environments, where many methods have been used, such as feedback controller, feed forward controller, and the hybrid controller. The existing active noise cancelling (ANC) systems use filtered-x least mean square (FxLMS) algorithm to continuously adjust the coefficients of the digital filter through a cost function based on the amount of noise measured. These ANC systems require high computational complexity, power intensive hardware, and significant processing time for measuring noise signal, and then calculating and synthesizing proper anti noise signals to cancel out the noise signals in real time. The theory of actively cancelling the noise is simple, but the realization of an efficient ANC system is challenging due to several physical constraints. Most of the previous studies provide only simulation results rather than physically measuring results and current commercialized ANC in-ear headphones can have extremely high prices compared with the common ones.

The ANC applications often use the high-speed digital signal processors (DSPs) to carry out the active noise cancellation systems. For example, an active noise cancellation system in a long duct was realized on DSP platform to achieve real-time performance in attenuating the narrowband noise at low frequencies efficiently. The adaptive feedback ANC algorithm and its variations have been proposed for the ANC headphones to cancel out the narrowband noise at low frequencies. To effectively cancel the broadband noise for the ANC headphones, Guldenschuh and Hold rich exploit a prediction filter to replace the LMS algorithm. Hence, the system did not require real-time updates and became more robust against the acoustic changes. However, Guldenschuh and Hold rich mainly depend on the passive attenuation of the headphones. This is quite different from the target for in-ear headphones. A simple and effective approach for designing feedback controllers had been proposed, which attenuated the broadband noise effectively based on analyzing the waterbed effect of the feedback ANC system. Zhang and Qui study the causality issue on a feed forward ANC headphone with different directions of noise sources in free field so that the system can effectively cancel the broadband noise.

Nevertheless, using DSP as a core component in the ANC systems, including, resulted in an expensive cost and high power dissipation. To reduce the cost for the ANC headphones, Chang and Li and Shyu et al. propose a modified feedback ANC algorithm and utilize a low-cost microcontroller unit as the core component in the ANC headphone. However, the noise cancelling performances of these systems become worse if the bandwidth of noise increases. In addition to stereo audio channels and high-performance/ low-power features, in-ear ANC headphones require stricter signal processing speed due to the physical constraints on the tiny volume. In this paper, a dedicated feed

forward ANC circuit implementation based on the well-known FxLMS adaptive algorithm for high

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fidelity in-ear headphones is developed. We have optimized the FxLMS adaptive algorithm with filter length exploration and proposed efficient hardware architecture for realizing the required convolution operations. By selecting a proper filter length, 62.7% of the computation complexity of convolution filter can be saved without sacrificing any ANC performance.

In addition, a dedicated storage mechanism called one-update circular buffer is proposed to keep the switching activity low to save power. Finally, a three-stage pipelining multiply accumulator (MAC) architecture is used to increase the data throughput. By adopting the standard cell-based VLSI design flow, the proposed design has been successfully implemented through using TSMC 90-nm CMOS technology. This new design possesses the features of using lower operating frequency and consuming much less power that facilitate better performance than the conventional ANC headphones. In addition, a systematic analysis is also presented to predict the performance of a typical feed forward single-channel ANC in-ear headphone in terms of the delay, which discloses that the noise reduction bandwidth is limited and maximum noise reduction is degraded with a longer delay between the noise and the anti noise signals. Moreover, the proposed design has been verified under versatile noise scenarios for its real time ANC performance by using a field-programmable gate array (FPGA) platform (XILINX ZEDBOARD). The proposed design can attenuate 15 dB for the pink noise with a broadband bandwidth of 50–1500 Hz. The goal of active noise cancellation (ANC) is to reduce the amplitude of the sound pressure level of the noise incident on the receiver or ear by "actively" introducing a secondary, out-of-phase acoustic field, “anti noise”. The resulting destructive interference pattern reduces the unwanted sound.

Over the past two decades, significant advances in control theory and the development of flexible, programmable, high-speed digital signal processing computers have made it possible to model and implement more complex active noise control systems. ANC is based on either feed forward control or feedback control. In feed forward control, a reference input coherent with the noise is sensed before it propagates past the secondary source. In feedback control, the active noise controller attempts to cancel the noise without the benefit of an “upstream” reference input. Structures for feed forward ANC are classified into (1) broadband adaptive feed forward control with a control field reference sensor, (2) narrowband adaptive feed forward control with a reference sensor that is not influenced by control field. Feed forward ANC is generally more robust than feedback ANC particularly when the feed forward system has a reference input isolated from the secondary anti noise source. NCHs rely on the passive acoustic isolation of headphones as well as ANC to provide broadband noise reduction as shown in Fig. Closed-ear headphones can passively block high frequency noise down to about 500Hz. At high

frequencies, a well designed closed-ear headphone can reduce noise by nearly 30dB - the amount of attenuation being dependent upon the quality of the seal from the ear cushion around the ears, the construction of the ear cups and the sound-absorbent materials used in the ear cups.

II. PROPOSED Fx LMS ANC SYSTEM

A. Design Considerations

A feed forward ANC control system uses an input microphone close to the noise source to pickup the noise signal x(n) before it is sensed by the listener. Accordingly, the ANC controller can produce an antinoise signal y(n) processing equal amplitude but opposite phase of x(n). Such antinoise signal is used to drive the cancelling-loudspeaker to generate a cancelling sound that attenuates the primary acoustic noise in the ANC system. Fig. 1 shows the application of the feed forward FxLMS adaptive algorithm in ANC system, where P(z) and S(z), respectively, denote the primary-path and the secondary-path models. In addition, W(z) indicates the filter weights of the ANC controller to adaptively generate the required antinoise signal according to the time-variant noise source. An available estimate of S(z) is represented by S’(z) in order to predict the noise signal that passed the secondary path. Among the signals shown in Fig. 1, e(n) is the error signal generated by acoustically combining the primary noise d(n) and the adaptive filter output y(n).

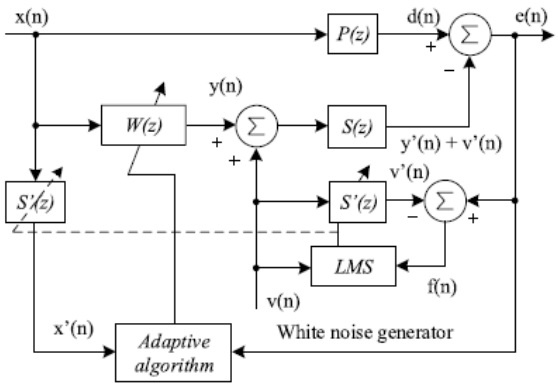

Fig. 1. Feed forward FxLMS algorithm.

The output y(n) of an adaptive filter at time n is given by

$$y(n) = \hat{w}^T(n)x(n) \quad \textbf{(1)}$$

where $\hat{w}(n) = [w_0(n)w_1(n)\ldots w_{L-1}(n)]^T$ is the L × 1 filter coefficient vector and $\mathbf{x}(n) = [x(n)x(n-1)\ldots x(n-L+1)]^T$ is the L × 1 reference signal vector. The FxLMS algorithm

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updates the weighting coefficients of the adaptive filter in a way as

$$\hat{w}(n+1) = \hat{w}(n) + \mu_1 x(n) * h(n) e(n) \quad (2)$$

where μ1 is the step size of the algorithm that determines the stability and convergence speed of the algorithm, h(n) is the impulse response of S(z), and e(n) is the error signal defined by

$$e(n) = d(n) - y(n). \quad (3)$$

The input vector x(n) is filtered by S(z) before updating the weighting vector. However, in practical applications, S(z) is unknown and must be estimated by S_(z). Therefore, the resulting FxLMS algorithm can be represented by

$$\hat{w}_l(n+1) = \hat{w}_l(n) + \mu_1 x'(n-l)e(n), \quad l = 0, 1, 2, \ldots, L-1 \quad (4)$$

where

$$x'(n) = \sum_{m=0}^{M-1} s'_m(n) x(n-m), \quad m = 0, 1, 2, \ldots, M-1 \quad (5)$$

X'(n), as shown in (5), indicates an estimated version of the reference input x(n) after passing through the secondary path

$$x'(n) = [x'(n) x'(n-1) \ldots x'(n-M+1)]^T \quad (6)$$

In addition, **s**' m(n) denotes each term of the coefficient vector of the estimated secondary path S(z)

$$s'_m(n) = [s'_0(n) s'_1(n) \ldots s'_{M-1}(n)]^T, \quad m = 0, 1, 2, \ldots, M-1 \quad (7)$$

The identification of secondary path is given as follows:

$$f(n) = e(n) - \sum_{m=0}^{M-1} s'_m(n) v(n-m) \quad m = 0, 1, 2, \ldots, M-1 \quad (8)$$

$$s'_m(n+1) = s'_m(n) + \mu_2 v(n-m) f(n) \quad m = 0, 1, 2, \ldots, M-1 \quad (9)$$

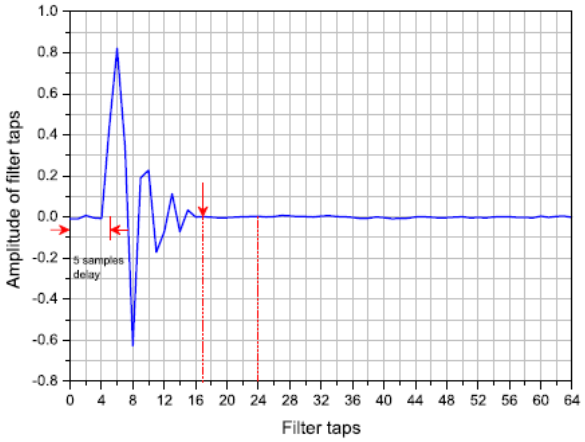

Fig. 2. Estimated secondary-path filter coefficients of S'(z) using white noise for offline modeling.

The feed forward FxLMS ANC algorithm introduced above is adopted to carry out a dedicated ANC circuit design for in-ear headphones. In the ANC headphone applications, the secondary path S(z) needs to be estimated and used in the updating stage of the FxLMS algorithm. Estimation is often performed offline. However, to keep track on the changes of S(z) due to small position variations of the in-ear headphone, an online modeling of S(z) is required [1], [17]. A model for either offline or online modeling is presented in Fig1, which is located at the output of the feed forward FxLMS ANC system. The offline modeling of S(z) is first realized to obtain the secondary path estimation S_(z) by using the white noise signal with a bandwidth of 20 Hz–20 kHz, where the sampling rate is set as 96 kHz and the step size is 0.01 for LMS algorithm. Fig. 2 shows the practical secondary-path filter coefficients in the in-ear headphone, where the total delay of the secondary path is around five samples. Besides, we can know from Fig. 2 that using a length of 24 taps is enough for modeling the secondary path of the in-ear headphone because all the amplitudes of filter coefficients approach zero after the 17th tap.

Moreover, using the impulse response with a longer length, e.g,64 tap, has been studied in [21]. Comparison between the proposed design and [21] shows that there is no obvious difference in noise reduction performance by using 24 tap or 64 tap. Furthermore, to verify the correctness of the estimated secondary-path transfer function S(z), an experiment using sound check testing machine was executed. As shown in Fig3, the magnitude response of S(z) using white noise closely matches that of S(z). In ANC systems, the primary-path delay must be greater than the total secondary-path delay to ensure that the feed forward adaptive filter has a causal response [9], [18]. The causality constraint is an extremely important condition; it directly affects both the maximum noise reduction and the attenuation bandwidth of a feed forward ANC headset. This even becomes more severe in in-ear headphones due to the physical and esthetic constraints on the tiny volume. In other words, the prototype in-ear headphone is equipped with an error microphone inside and a reference microphone outside each ear-cup, where the error microphone is only 1.5 cm away from the reference microphone, which is about one-third of that in ANC earmuff headsets (e.g., it is 5 cm [9]).

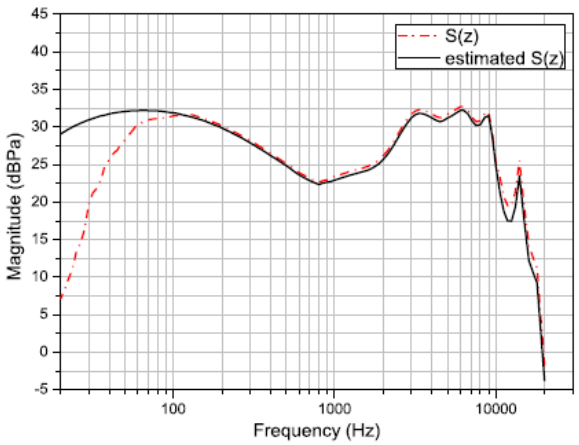

Fig. 3. Magnitude responses of both S(z) and S'(z)

using white noise as excitation signals. Dashed-dotted line: S(z). Solid line: estimated S'(z).

This means that the acoustic delay of the primary path was narrowed significantly against its total electrical system delay, which results in that the causality constraint may be easily violated in in-ear headphones. Because this design concentrates on the digital design of the ANC signal processing, we adopt commercial analog to- digital and digital-to-analog converters equipped on the FPGA platform to realize the mixed signal processing. On the platform, only two kinds of sampling frequencies, i.e., 48 and 96 kHz are available so that we use a sampling frequency of 96 kHz for the proposed ANC in-ear headphone. The primary source is placed 35 cm away from the ear-cup, to ensure that the direct sound field is dominant. The signals measured by the reference microphone and error microphone are, respectively, indicated by x(n) and d(n). These signals x(n) and d(n) are then used to identify the primary path, where the primary-path delay between two primary source locations is estimated to be six samples and four samples for 0° and 90° positions, respectively. The experimental installation for identifying the primary-path filter with two different primary source locations is shown in Fig. 4. Before implementing the proposed design, a systematic analysis is presented to predict the noise reduction performance of the prototype feed forward ANC in-ear headphone through adopting the following two tests: 1) playing broadband pink noise at 0° position and 2) playing broadband pink noise at 90° position.

In this paper, we adopt 24-tap filters for both W(z) and S(z). Step size of 0.01 was used in the adaptive filter W(z). In online modeling, the small step size of 0.004 should be kept to adapt effectively to the small changes of S(z). Fig4 shows the noise cancelling performance of the proposed design in the frequency domain, where the solid line indicates the original noise signal, the dashed-dotted line illustrates the attenuated sound signal measured in the acoustic cavity when the ANC controller is turned-ON, and the vertical axis indicates the magnitude of noise. Fig4(a) shows the predicted performance of the ANC in-ear headphone with the noise source at 0° position, where the proposed design performs well in reducing broadband pink noise at a bandwidth of 40–1500 Hz, with a noise reduction of 17 dB. Meanwhile, Fig4(b) shows the predicted performance of the ANC in-ear headphone with the noise source located at 90° position. From Fig4(b), we can find that the maximum noise reduction achievable is ~12dB and the attenuation bandwidth reaches 900Hz. Compared with the predicted results for the primary source at 0° position, as shown in Fig4(a), the maximum noise decreases ~5dB, and the attenuation bandwidth narrows ~600Hz. The analysis on the delay of the primary and secondary paths shows that the primary-path delay decreases in two samples after the primary source changes from 0° position to 90° position, which leads to the noncausality of the ANC in-ear headphone.

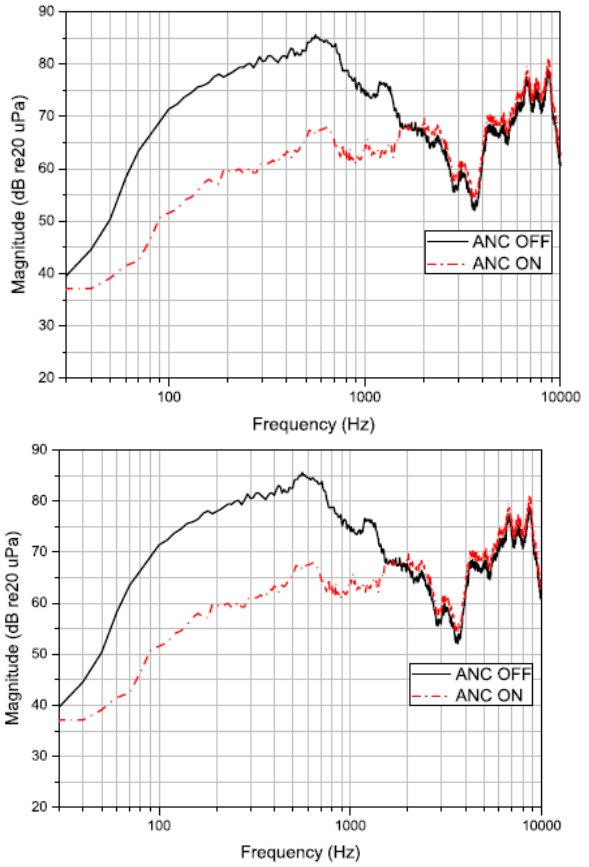

Fig4. Power spectral density of the feedforward ANC in-ear headphone. Solid line: ANC OFF. Dashed-dotted line: ANC ON. (a) Primary source at 0° position. (b) Primary source at 90° position.

B. Proposed Architecture for the ANC In-Ear Headphone

Fig6 shows the system architecture for implementing the proposed ANC system prototype where the proposed ANC architecture is shown in the bottom half of the figure. The rest of the platform, such as the ARM cortex-A9 processor, the AXI4 interconnect block, and the I2S audio CODEC, is used to realize the ANC system prototype. The ARM processor is only responsible for allocating tasks to each module of the system. As shown in Fig5, the proposed design contains the following submodules: 1) two 24-tap adaptive filters, i.e., LMS_24_tap_W(z) for producing the antinoise signal y(n) and LMS_24_ tap_S_(z) for estimating the secondary path online; 2) a finite-impulse response (FIR) filter, i.e., S_(z)_F I R_24_tap_x_(n), to produce the signal x_(n) that is a filtered version of the signal x(n); 3) an adder for summing up the antinoise signal y(n) and the additive white noise used to keep track on the changes of S(z) due to small position variations of the in-ear headphone; and 4) an I2S block in order to receive and

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transmit the data from the feed forward FxLMS ANC circuit to the I2S audio CODEC.

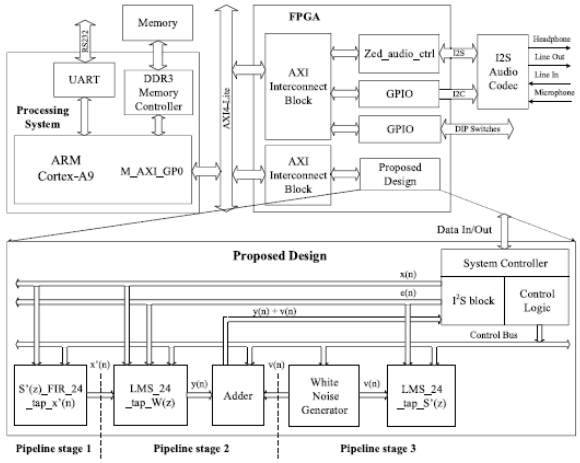

Fig5. Top-level block diagram of the system architecture.

For digital signal processing systems that require low-power consumption, throughput capability is an important design factor except area and operating frequency. Although DSP microprocessors provide high programmability, the serial processing manner and the iterative computation result in low efficiency. In contrast to a single processing unit, a parallel architecture involving more hardware MAC units uses custom logic design can bring a higher throughput. However, this technique requires the cost of increased logic complexity, chip area usage, and power consumption [22]. Besides, the optimized VLSI design must be able to cancel the broadband noise at the same time. Therefore, we optimize the ANC system with strategies specialized in terms of speed, area, and power dissipation in terms of the following design phases.

1. Identifying the Computational Intensity Parts: The major computational burden is composed of three convolutions. The first one is for the calculation of control filter and the rest two are, respectively, for updating the coefficients of S(z) and obtaining the estimate x(n). Because the hardware complexity grows proportionally with the number of the filter length, we tend to first analyze the adopted algorithm and find out an optimized filter length for implementing the ANC design. Moreover, an important part for realizing the convolutions in ANC applications is that we need a buffer to store the previous values along with the current sample. Whenever a new sample enters the buffer, all the values need to be shifted forward with one entry of space. This causes the redundant processing overhead for the whole system, especially for the filters with a long length. We propose a one-update circular RAM buffer that only one entry of the buffer needs to be updated with a new value when a new sample is acquired from the input port. We have more details about this buffer in the following.

2. Designing the Efficient Convolution Operation

Unit: To save resources and clock cycles, we adopted a sequential filter structure for FIR filter by using single-multiplier MAC unit. Besides, we utilize fully pipelined architectural design to speed up the throughput of this design. Altogether, we show that our proposed design is more suitable in terms of both power consumption and noise reduction performance for in-ear headphones. The associated data samples are stored in the buffer; whenever a new sample enters the delay line, all the values need to be moved down the delay line and the new sample enters the recently vacated position at the top of the buffer. This causes the redundant processing overhead for the whole system. Therefore, we propose the one-update circular buffer in which only the oldest value is replaced by the newest sample and keep the rest values the same. In such manner, the switching activity of the buffer can be kept in a very low level so that much power consumption can be saved. Moreover, the control and the addressing are also very simple. The memory organizations of both coefficients and samples are shown in Table II, where w and x indicate the filter coefficient and data sample, respectively. The address generator needs only to supply sequential addresses and only one value needs to be changed when a new sample arrives. Examples for calculating the outputs of 24-tap FIR filter using the circular buffer are shown as follows:

$$y[23] = w[0]x[23] + w[1]x[22] + \cdots + w[23]x[0] \quad (10)$$

$$y[24] = w[0]x[24] + w[1]x[23] + \cdots + w[23]x[1] \quad (11)$$

$$y[25] = w[0]x[25] + w[1]x[24] + \cdots + w[23]x[2] \quad (12)$$

$$y[26] = w[0]x[26] + w[1]x[25] + \cdots + w[23]x[3]. \quad (13)$$

Two counters are equipped to drive the addresses of the data buffer and coefficient buffer. The input data and the coefficients of filter are, respectively, stored in the proposed one-update circular data buffer and the coefficients buffer stores. Besides, we adopt a three-stage pipelining MAC architecture to increase the data throughput rate of the MAC FIR filter, as shown in Fig9. In each cycle, the data and the coefficients are read from the interleaving buffers to the registers. Then, the multiplication of the two operands of the convolution is performed and one adder then accumulates the partial products to generate the result of the convolution operation. The output of FIR filter S(z) appears every M+4 cycles. Such architecture is much more efficient than using microcontrollers or DSPs. When using a PIC24H processor or a DSP, the convolution implementation, i.e., a multiplication and

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an addition requires 2M cycles to finish all calculations. Hence, for the required sampling rate of 96 kHz, the optimal operating frequency is reduced from 40 to 20 MHz, and a 50% power saving may be reached. The controller in Fig.9 provides the necessary addresses and control signals to the data path. It includes two counters.

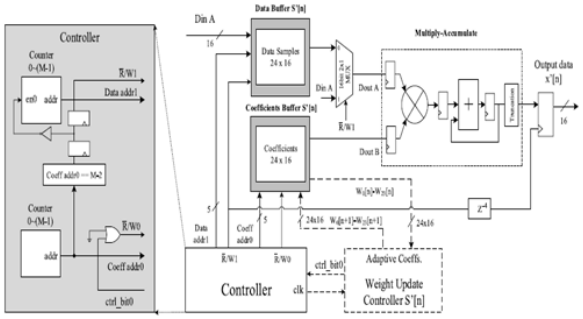

Fig6. Pipelined single-multiplier MAC FIR filter structure of the FIR filter S (z).

One counter controls the address of the filter coefficients, This signal must be delayed to ensure that the latency on the signal matches with the latency through the MAC engine. These data RAM buffers are used to store the input data x(n), the adjusted coefficients of adaptive algorithm w(n), and the output data of the estimate FIR filter x(n), respectively. The proposed hardware architecture not only possesses high computing performance but also owns good flexibility to generate suitable anti noise signal adaptively. Three counters are used to provide the necessary addresses for the data buffer x[n], data buffer x[n], and coefficients buffer w[n], respectively. This module uses the LMS algorithm followed by using the white noise generator v(n) as the reference input to adjust the weights online. It contains the MAC FIR filter and two data RAM buffers. These data RAM buffers are used to store the input data v(n) and the adjusted coefficients of the secondary-path estimation S(z).

III. SIMULATION RESULTS

The proposed design has been implemented through using a standard cell-based design flow and fabricated by using the TSMC 90-nm CMOS technology. Besides, it has been completely verified on an FPGA platform. The details of VLSI implementation of the proposed work are presented in the following paragraphs. Because the operating frequency of the proposed design is chosen as 20 MHz, the proposed design has to finish the signal conversion and all calculations within 208 clock cycles. Meanwhile, the proposed design only takes 134 clock cycles to finish the computations, in which 28 cycles are to realize the operation of the secondary path, the other 28 cycles are to calculate the output of the adaptive filter, 25 cycles are to update the coefficients of the adaptive filter, and the final 53 cycles are used to update the coefficients of the secondary-path estimation S(z). The exceeded computing power makes the proposed design capable of collaborating with higher frequency data converters.

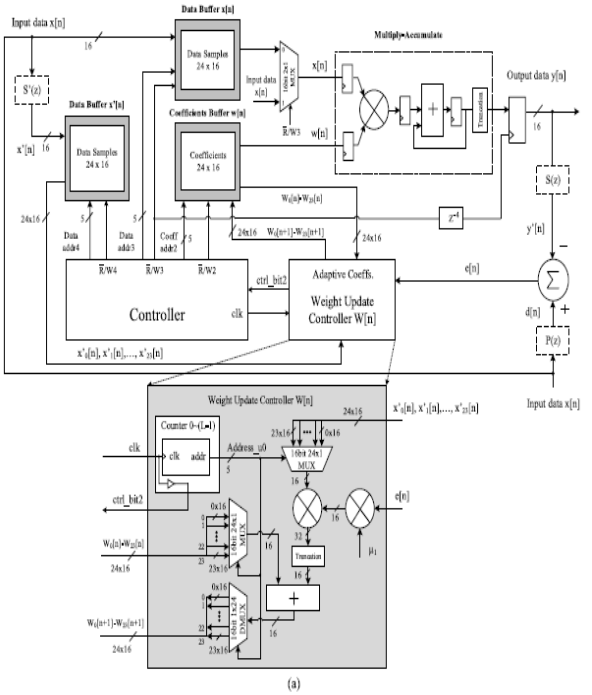

Fig7. Proposed 24-tap pipelined LMS filter architecture.

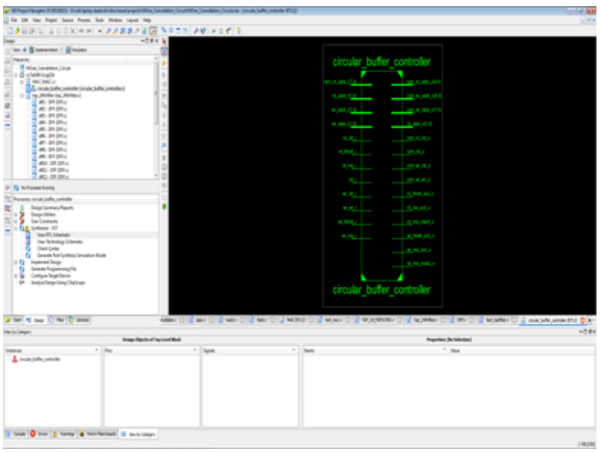

Fig8. RTL Schematic

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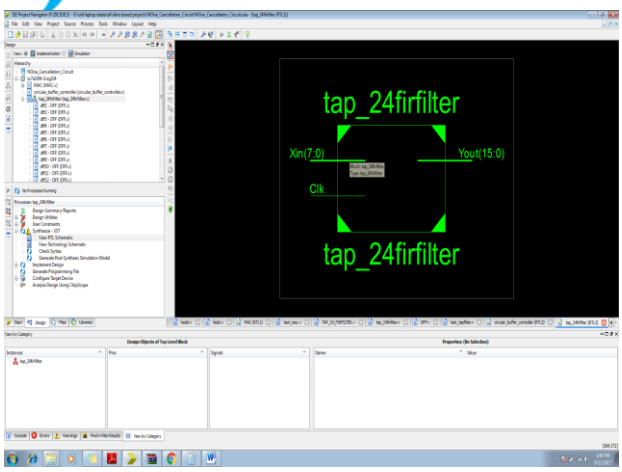

Fig9. RTL Schematic of Tap Filter

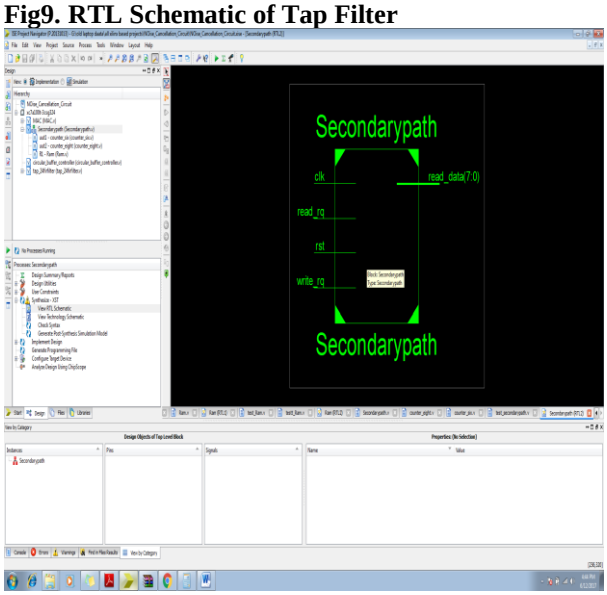

Fig10. Secondary path RTL Schematic and Waveforms

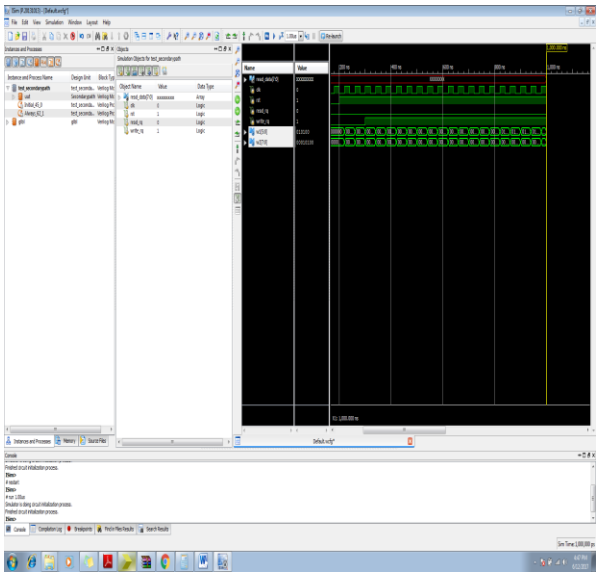

Fig11. Simulation Result

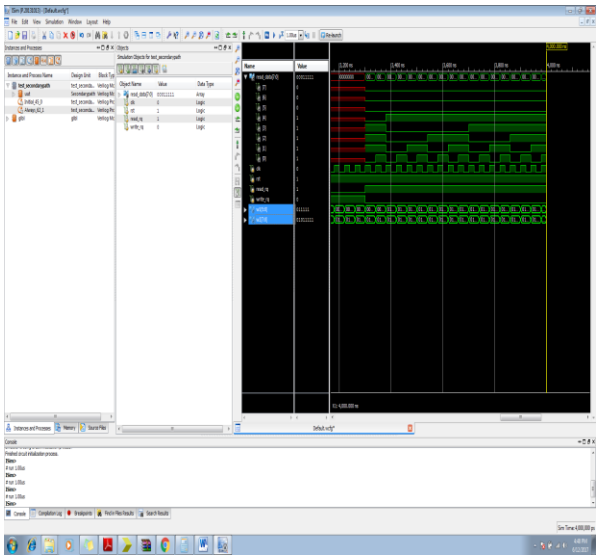

Fig12. When read signal is 0 and write signal is 1 ,then only the data stores inside the ram but it wont show in output.

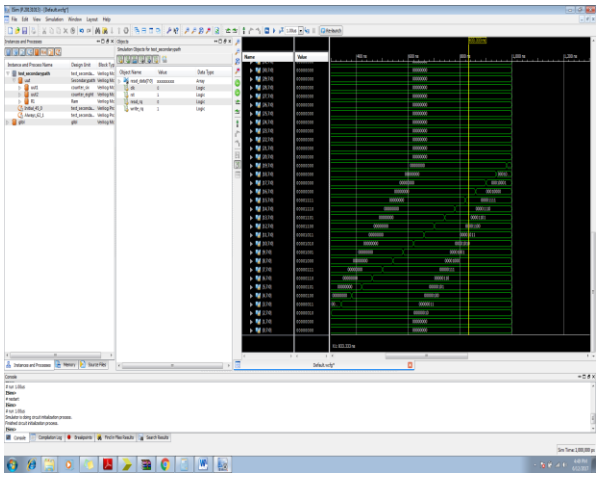

Fig13. When read request is 1 and the output shows the results in read data stage.

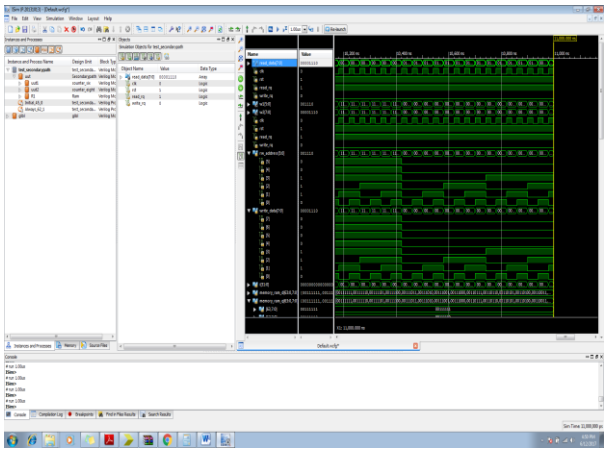

Fig14. Memory stores a values.

V. CONCLUSION

In this paper, an area-/power-efficient feed forward FxLMS ANC circuit has been developed for in-ear headphones. The proposed design has been successfully implemented by using TSMC 90-nm CMOS technology. To verify the validity of the proposed design, a series of physical measurements has been executed in an anechoic chamber. Furthermore, the measurement results were compared with that of other state-of-the-art works. The experimental results show that the proposed high-performance/low-power ANC circuit design can reduce disturbing noise of various frequency bands very well, and outperform the existing works. The proposed design can attenuate 15 dB in physical measurement for the broadband pink noise between 50 and 1500 Hz when operated at 20-MHz clock frequency at the cost of 84.2 k gates and a power consumption of 6.59 mW only.

VII. REFERENCES

[1] S. M. Kuo and D. R. Morgan, "Active noise control: A tutorial review,"Proc. IEEE, vol. 87, no. 6, pp. 943–973, Jun. 1999.
[2] S. M. Kuo, I. Panahi, K. M. Chung, T. Horner, M. Nadeski, and J. Chyan,"Design of active noise control systems with the TMS320 family,"Texas Instruments, Stafford, TX, USA, Tech. Rep. SPRA042,Jun. 1996.
[3] L. Wu, X. Qiu, and Y. Guo, "A simplified adaptive feedback active noise control system," Appl. Acoust., vol. 81, pp. 40–46, Jul. 2014.
[4] W. S. Gan, S. Mitra, and S. M. Kuo, "Adaptive feedback active noisecontrol headset: Implementation, evaluation and its extensions," IEEE Trans. Consum. Electron., vol. 51, no. 3, pp. 975–982, Aug. 2005.
[5] Y. Song, Y. Gong, and S. M. Kuo, "A robust hybrid feedback active noise cancellation headset," IEEE Trans. Speech Audio Process., vol. 13, no. 4,pp. 607–617, Jul. 2005.
[6] S. M. Kuo, S. Mitra, and W.-S. Gan, "Active noise control system for headphone applications," IEEE Trans. Control Syst. Technol., vol. 14,no. 2, pp. 331–335, Mar. 2006.
[7] M. Guldenschuh and R. Höldrich, "Prediction filter design for activenoise cancellation headphones," IET Signal Process., vol. 7, no. 6,pp. 497–504, Aug. 2013.
[8] L. Zhang, L. Wu, and X. Qiu, "An intuitive approach for feedback activenoise controller design," Appl. Acoust., vol. 74, no. 1, pp. 160–168,Jan. 2013.
[9] L. Zhang and X. Qiu, "Causality study on a feedforward active noisecontrol headset with different noise coming directions in free field,"Appl. Acoust., vol. 80, pp. 36–44, Jun. 2014.
[10] C.-Y. Chang and S.-T. Li, "Active noise control in headsets by using a low-cost microcontroller," IEEE Trans. Ind. Electron., vol. 58, no. 5,pp. 1936–1942, May 2011.
[11] K.-K. Shyu, C.-Y. Ho, and C.-Y. Chang, "A study on using microcontroller to design active noise control systems," in Proc. IEEE Asia Pacific Conf. Circuits Syst. (APCCAS), Nov. 2014, pp. 443–446.
[12] S. Hu, R. Rajamani, and X. Yu, "Invisible speakers in home windows for simultaneous auxiliary audio playback and active noise cancellation," Mechatronics, vol.22, no.8, pp. 1031–1042, Dec. 2012.
[13] S. Hu, R. Rajamani, and X. Yu, "Directional cancellation of acoustic noise for home window applications," Appl. Acoust., vol. 74, no. 3,pp. 467–477, Mar. 2013.
[14] T. Pàmies, J. Romeu, M. Genescà, and R. Arcos, "Active control of aircraft fly-over sound transmission through an open window," Appl.Acoust., vol. 84, pp. 116–121, Oct. 2014.
[15] I.-H. Yang, J.-E. Jeong, U.-C. Jeong, J.-S. Kim, and J.-E. Oh, "Improvement of noise reduction performance for a high-speed elevator using modified active noise control," Appl. Acoust., vol. 79, pp. 58–68,May 2014.
[16] P. Peretti, S. Cecchi, L. Romoli, and F. Piazza, "Adaptive feedback active noise control for yacht environments," IEEE Trans. Control Syst.Technol., vol. 22, no. 2, pp. 737–744, Mar. 2014.
[17] S.-C. Chan and Y. Chu, "Performance analysis and design of Fx LMS algorithm in broadband ANC system with online secondary-path modeling, "IEEE Trans. Audio, Speech, Lang. Process., vol. 20, no. 3,pp. 982–993, Mar. 2012.
X. Kong and S. M. Kuo, "Study of causality constraint on feed forward active noise control systems," IEEE Trans. Circuits Syst. II, AnalogDigit. Signal Process., vol. 46, no. 2, pp. 183–186, Feb. 1999.
[19] PIC24H Family Data Sheet. High-Performance, 16-BitMicrocontrollers.[Online].Available:http://www.microchip.com/downloads/en/DeviceDoc/70175d.pdf, accessed Jan, 2015.
[20] The Power Consumption of the Texas Instruments C6748/46/42.[Online].Available:http://processors.wiki.ti.com/index.php/C6747/45/43_Power_Consumption_Summary, accessed Jan, 2015.
[21] H.-S. Vu, K.-H. Chen, S.-F. Sun, T.-M. Fong, C.-W. Hsu, and L. Wang,"A power-efficient circuit design of feed-forward FxLMS active noise cancellation for in-ear headphones," in Proc. Int. Symp. VLSI Design, Autom. Test (VLSI-DAT), Apr. 2015, pp. 1–4.
[22] D. Allred, V. Krishnan, W. Huang, and D. Anderson, "Implementation of an LMS adaptive filter on an FPGA employing multiplexed multiplier architecture," in Proc. Conf. Rec. 37th Asilomar Conf. Signals, Syst.Com put., Nov. 2003, pp. 918–921.