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CDTA Based Analog Multiplier

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***Abstract*— A CDTA (current differencing transconductance amplifier) based analog multiplier has been proposed with no usage of the passive components however three MOS transistors have been connected externally. Some of its main features include a low working voltage and suitable for integration operations with no externally connected passive component. The proposed work has been verified on 0.18um technology and the performance simulation results have been shown.**

***Keywords*—CDTA, Active Building Block, FVF, Multipier etc.**

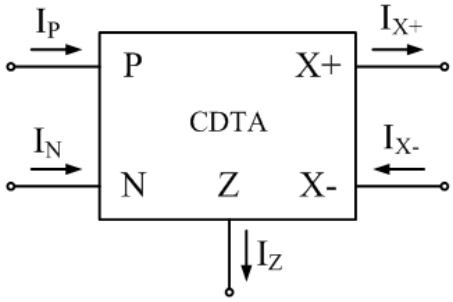
I. INTRODUCTION

Even though the world has been digitized to a good extent however the natural signals are analog in nature. In order to make the devices area efficient and portable it become necessary to lower the operating voltages so that the battery lasts for a loner time thus there is a need for development of low voltage analog signal processing blocks. Although in the recent years a large number of ABB (Active Building Blocks) were proposed for analog signal processing, still there is a scope for development of new active elements that have better advantages to offer. This work focuses on current mode CDTA and its application as an analog multiplier.

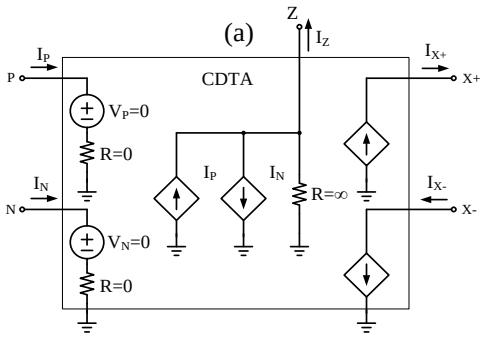
CDTA is an active building block that has a large operating range of frequency due to its current mode operation [1-2]. With CDTA as a basic building block it is possible to design a circuit with few or no use of passive components than its other counterparts like CDBA (Current Differencing Transconductance Amplifier). Also it is a five terminal device hence a circuit requires less number of blocks and thus making the structure overall area efficient. The simulation results of CDTA have been obtained in PSPICE and to make a good use of its advantages a multiplier has been also verified that operates at a low voltage of 0.6v shown in Section III.

II. CDTA

Current differencing transconductance amplifier is a five terminal current mode class of active block that has a wide range of features and can be employed in designing of analog signal processing circuits especially filters. CDTA is considerably free off input parasitic resistances and capacitances and due to its current mode operation it has a wide operating frequency range [3]. Various current mode and voltage mode circuits have already been developed by various researchers particularly in the area of frequency filtering that include biquad circuits, higher order filters, all pass sections [4-6], gyrators, grounded and floating inductors and ladder structures [7-8]. A large number of signal generating blocks were developed that include high frequency oscillators [9-10], precise wave rectifiers, Schmitt trigger etc.



(a)



(b)

$$\begin{bmatrix} I_Z \\ I_{X+} \\ I_{X-} \\ V_P \\ V_N \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 1 & -1 \\ gm & 0 & 0 & 0 & 0 \\ -gm & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} V_Z \\ V_{X+} \\ V_{X-} \\ I_P \\ I_N \end{bmatrix}$$

(c)

Fig. 1: (a) Block diagram of CDTA, (b) Ideal Model of CDTA, (c) Functional matrix of CDTA

A) BASIC OPERATION of CDTA

The schematic symbol of CDTA is shown in figure 1. It consists of a pair of current input terminals p and n with low impedance and z as an auxiliary terminal in which the amount

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of current is the difference of the two input currents. The output currents are equal in magnitude but flow in opposite direction and are equal to the product of the g_m of the dual output OTA and voltage at terminal z. Hence the CDTA characteristic equations are defined as follows:

$Vp = Vn = 0,$
$Iz = Ip - In,$
$Ix + = gm.Vz,$
$Ix - = - gm.Vz.$

Where $Vz = Iz.Zz$ and Zz is an external impedance connected at z terminal.

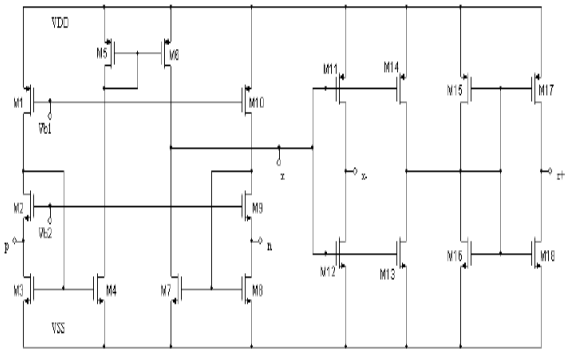

Fig. 2 : CMOS realization of CDTA

The MOSFET configuration of CDTA is shown in figure 2 as given in [12]. The input stage of the CDTA is constructed by transistors M1 to M10. Flipped voltage followers (FVF) have been used in the current mirrors. The advantage of using FVF is that it provides a low input resistance. The resistance of terminals p and n used as the output resistance of FVF. M2, M3 M8 and M9 constitute the FVF transistors. The resistance of input terminals of CDTA and output resistance of FVF is of the order of tens of ohms.

The aspect ratios of all the MOSFET's used in designing of CDTA are mentioned in table 1.1. it is quite evident from the table that the length of the transistors used in current mirrors is kept large than rest of other transistors in order to counter the channel length modulation effect which causes a DC offset at the input stage.

M1=3.6µ/1.8µ	M9=3.6µ/1.8µ
M2=3.6µ/1.8µ	M10=4µ/1.4µ
M3=3.6µ/1.8µ	M11=10µ/0.7µ
M4=3.6µ/1.8µ	M12=4µ/1.4µ
M5=3.6µ/1.8µ	M13=10µ/0.7µ
M6=3.6µ/1.8µ	M14=4µ/1.4µ
M7=3.6µ/1.8µ	M15=10µ/0.7µ
M8=3.6µ/1.8µ	M16=4µ/1.4µ

Table 1.1: Aspects of Transistors

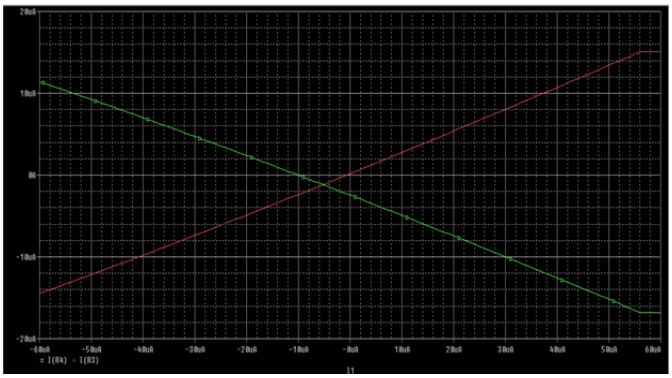

Fig. 3: Variation of z terminal current w.r.t input current

It can be observed from figure 3 that after a DC current of 56µA the current remains constant and its value can be easily increased by enhancing the bias currents of current mirror transistors. This increase in bias current certainly also increases the total power dissipation.

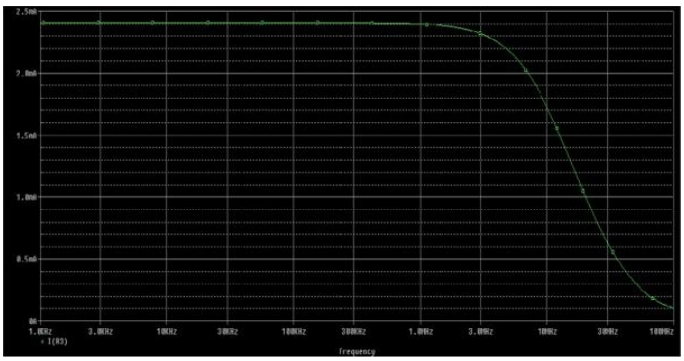

Fig. 4: Variation of n terminal current Vs Frequency

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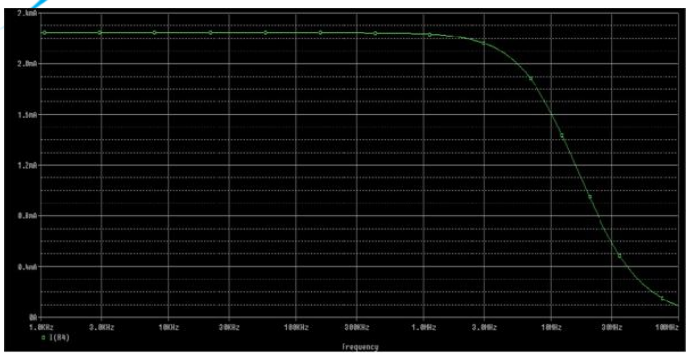

Fig. 5: Variation of p terminal current Vs Frequency

Supply Voltage	±0.6v
Bias Current	56µA
Technology	0.18µ MOSIS
Power Consumption	0.37mW
Transconductance	210µA/V
Biasing Voltages	Vb1=0.9v
Input Offset Current	0.4µA

TABLE SUMMARY OF SIMULATION RESULTS

III. PROPOSED WORK

In modulation, measurement and instrumentation and control systems analog multipliers are used extensively [4-16]. Many techniques to implement multipliers are available in literatures such as multiplier based on translinear property of BJT [17] and square law property of CMOS circuits [18], suing switched capacitor (SC) and four quadrant multiplier using CDBA [19]. In biomedical equipments CDTA based precision rectifiers are employed. In this section a new multiplier using single CDTA and three MOSFETS have been proposed. This analog multiplier circuit performs the multiplication of two bipolar signals Vx and Vy in real-time and produces an output Vo = k(Vx, Vy). The differential nature of CDTA due to current differencing unit makes it suitable for analog signal processing applications that demand high bandwidth, high speed and a simple implementation.

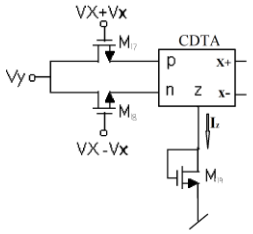

Fig.6: Analog Multiplier

In the configuration shown in figure 6 MOSFETS M17 and M18 are matched pairs, M17 and M18 work in the linear region while the latter work in saturation region. The drain current of a simple MOS transistor is given by the equation is given by:

$$I_d = \mu.c_{ox}.(w/l).(V_{gs}-V_t-V_{ds}/2).V_{ds} \quad \ldots\ldots(1)$$

Where Vt <= Vgs- Vds, Vgs > Vt for n channel MOSFET, Vt is the threshold voltage of the MOSFET while u, Cox, w, l stand for carrier mobility, oxide layer capacitance, width of the transistor and length of the transistor respectively [14]. In this figure Vx and Vy are the time varying voltage signals while Vx is the bias voltage and CDTA keeps the sources of the two MOSFETS (M17 &M18) virtually grounded. Here the output currents are obtained from the drain current equation (1) where:

$V_{gs} = VX+Vx$ and $V_{ds} = Vy$, with

$KM17= KM18= K,$

$Ip = K\,(VX + Vx - VT - Vy/2).Vy$

$In = K\,(VX - Vx - VT - Vy/2).Vy$

The z terminal provides the difference of the two currents as:
$Iz = Ip - In = 2K.Vx.Vy$

Hence output voltage,
Vo = Iz.Z
Where z is transconductance (gm) of the transistor M19.
So Vo = 2K.Vx.Vy.gm

IV. SIMULATION RESULTS AND DISCUSSION

The above theoretically verified analog multiplier is designed and verified using PSPICE and model parameters of 1.8u provided by MOSIS. The CDTA used in this design has been realized with CMOS technology is already given in section 2. M18 and M 18 are selected to be identical NMOS transistors with 5u/5u and MOS M19 resistance is designed using NMOS

with aspect ratio of 10.8u/72u. The power supply is VDD= -VSS= 0.6V. A 10kHz voltage signal Vy with 1.2Vp-p amplitude is multiplied by 1kHz Vx with 1.2Vp-p amplitude.

The simulation results obtained in fig 7 and fig 8 have been found quiet close to the theoretical results. The discrepancies in the deviated behavior are due to non-zero input resistances, non-linearities of MOS transistors and parasitic capacitances and z terminal. However these effects can be minimized by modifying the aspect ratios of the transistors.

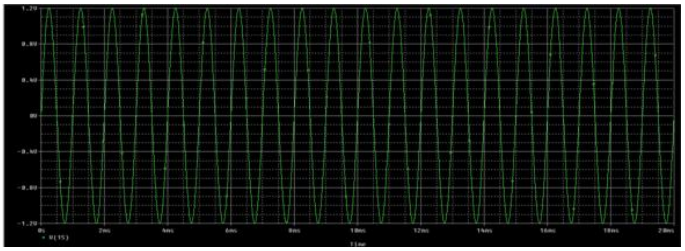

Fig. 7 1 kHz voltage signal Vx 1.2 Vp-p amplitude

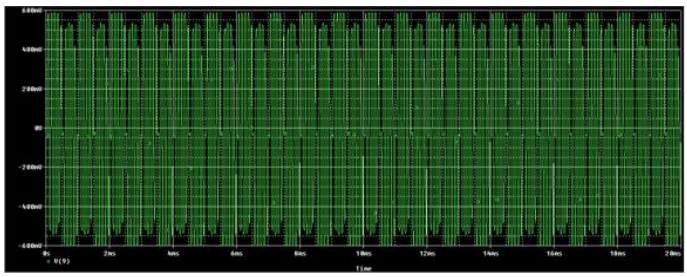

Fig.8- Resulting multiplication signal of Analog multiplier

V. CONCLUSION

A CDTA based analog multiplier is proposed and simulations results are obtained using PSPICE. The multiplier consists of a single CDTA and three externally connected MOS transistors and provides single ended voltage. Compared to operational amplifier where resistors along with two squaring circuits are employed to do the multiplication operation CDTA proves to be a better choice to be used as a multiplier. The multiplication factor is controlled by K.

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