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A Novel Approach for VHDL Implementation of Universal Line Encoder for Communication

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Abstract: This paper describes the implementation of various line coding schemes using VHDL on a single chip and enables the user to select one of them for the purpose of security, area optimization and can support communication in varying channel environment. The choice of line code depends upon presence or absence of DC level, power spectral density, bandwidth, BER performance, ease of clock signal recovery and presence or absence of inherent error detection property. The line encoding schemes used are Unipolar RZ and NRZ, Polar RZ and NRZ, AMI and Manchestor codings. Select pin impinged on the chip enables the users to select any one of the line encoding technique according to their requirement. The waveforms of Universal Line Encoder are presented using Modelsim 6.4.

Keywords: AMI (Alternate Mark Inversion), Line Encoding, NRZ (Non Return to Zero).

1. INTRODUCTION

After the emergence of VLSI technology, researchers are continuously trying to implement various algorithms by using VHDL or Verilog[1–9] but power, area optimization and reduction of time delay are big challenges in front of engineers[10]. Line encoding is key building block of communication system in which binary 1's and 0's are translated into a sequence of voltage pulses that can be propagated over wire[11]. Digital baseband signals often use line codes to provide particular spectral characteristic of a pulse train. Most popular codes are return to zero and non return to zero. All of these may be either unipolar, polar or bipolar. The choice of line code depends upon presence or absence of DC level, power spectral density, bandwidth, BER performance, ease of clock signal recovery and presence or absence of inherent error detection property[12]. RZ implies that pulse return to zero within every bit period. This leads to spectral widening but improves timing synchronization. NRZ codes, on the other hand do not return to zero in a bit period — the signal stays at constant level throughout a bit period. NRZ codes are more spectrally efficient than RZ codes, but offer poorer synchronization capabilities[13]. Unipolar encoding is inexpensive to implement but its average amplitude is nonzero, this creates a direct current (DC) component. Average DC value is minimum in polar formats as well as there is no signal droop[14] but they are not transparent. Manchester codes are self synchronizing but they have no error detection capability, so are not suitable for wide area network.

2. ALGORITHM

Signed binary notation is used to implement this design as explained in table (*A* and *B*). Xilinx Project Navigator is used to implement this design[15].

Table A

Line encoding technique	*Input (x)*	*Output (y) $(0 - T_b/2)$*	*Output(y) $(T_b/2 - Tb)$*
Unipolar-RZ	0	00	00
	1	01	00
Unipolar_NRZ	0	00	00
	1	01	01
Polar_RZ	0	11	00
	1	01	00
Polar_NRZ	0	11	11
	1	01	01
Manchestor	0	11	01
	1	01	11

Table B
Truth Table for AMI

Present state	*Input (x)*	*Output $(y_0 y_1)$*	*Next state*
0	0	00	0
0	1	01	1
1	0	00	1
1	1	11	1

3. MODELSIM SIMULATION RESULT

Modelsim 6.4 is used to see the waveforms of the project as shown in Figs (1 and 2). In this model select pin is used to change line encoding technique. In these waveforms the delay of 1 clock is observed.

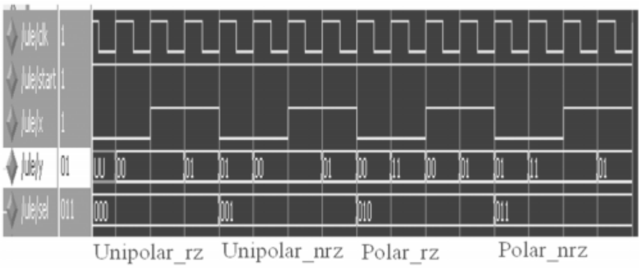

Fig. 1

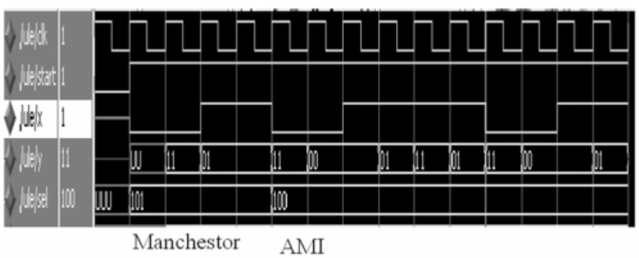

Fig. 2

4. CONCLUSION

The waveforms of Universal Line Encoder are presented using Modelsim 5.4 and confirm very well to the theoretical findings. Thus Universal Line Encoder can be built on a single chip enabling the user to select any of the line code schemes thereby eliminating each single chip for each code scheme. This technology is secure, compact in size and channel efficient. The procedure involved to build this encoder ease the test application processes and allow high level control for communication. The approach to develop algorithm for universal line encoder is quite simple and suitable for testing real life applications in communication.

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