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DESIGN AND IMPLEMENTATION OF LOW POWER MULTIPLIER USING VEDIC MULTIPLICATION TECHNIQUE

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ABSTRACT

In this paper a low power Multiplier is presented. The multiplier implemented here is based on the ancient Vedic Multiplication Technique. The Urdhva-tiryakbhyam and Nikhilam sutras are used for multiplication. The multiplier based on ancient technique is compared with the modern multiplier to highlight the power and speed advantages in the Vedic Multipliers. The Vedic Multiplier is tested by using BIST (Built In Self Test) and it is found Fault free. The results are compared with the Booth's Multiplier in terms of time delay and power. The high speed processor requires high speed and low power multipliers and the Vedic Multiplication technique is very much suitable for this purpose.

Keywords: Vedic multiplication, Urdhva-tiryakbhyam, Nikhilam, BIST.

1. INTRODUCTION

Multipliers are extensively used in FIR filters, Microprocessors, DSP and communication applications. For higher order multiplications, a huge number of adders or compressors are to be used to perform the partial product addition. The need of low power and high speed Multiplier is increasing as the need of high speed processors are increasing. The Vedic multiplication technique is based on 16 Vedic sutras or aphorisms, which are actually word formulae describing natural ways of solving a whole range of mathematical problems [1]. The mathematical operations using, Vedic Method are very fast and requires less hardware, this can be used to improve the computational speed of processors. In this paper we have implemented the Vedic multiplier in VHDL.

The paper describes the basic design and implementation of the Vedic Multiplier using Urdhva-tiryakbhyam and Nikhilam sutras. The paper is organized as follows. Section 2 describes the basic methodology of Vedic multiplication technique and Section 3 describes the implementation methodology and testing of Multiplier using BIST and section 4 comprises of Result and conclusion.

2. VEDIC MULTIPLICATION TECHNIQUE

The ancient Vedic multiplication techniques are equally applicable for binary numbers also. The Vedic mathematics reduces the cumbersome-looking calculations in conventional mathematics to a very simple one. This is so because the Vedic formulae are claimed to be based on the natural principles on which the human mind works. The proposed multiplier is based on Urdhva-tiryakbhyam - (Vertically and crosswise) sutra.

2.1 Urdhva-Tiryakbhyam Sutra

The Urdhva-tiryakbhyam sutra is basically vertically and crosswise. In this method the partial products are generated simultaneously which itself reduces the delay makes this method fast. The method is explained below for two, three bit numbers A and B where $A = a2a1a0$ and $B = b2b1b0$ as shown in Figure 1. Firstly, the least significant bits are multiplied which gives the least significant bit of the product (vertical). Then, the LSB of the multiplicand is multiplied with the next higher bit of the multiplier and added with, the product of LSB of multiplier and next higher bit of the multiplicand (crosswise). The sum gives second bit of the product and the carry is added in the output of next stage sum, which is obtained by processing the three bits with crosswise and vertical multiplication and addition to give the sum and carry. The sum is the corresponding bit of the product and the carry is again added to the next stage multiplication and addition of two bits except the LSB. The same operation continues until the multiplication of the two MSBs to give the MSB of the product [2,3].

$$s0 = a0b0; \quad (1)$$

$$c1s1 = a1b0 + a0b1; \quad (2)$$

$$c2s2 = c1 + a2b0 + a1b1 + a0b2; \quad (3)$$

$$c3s3 = c2 + a1b2 + a2b1; \quad (4)$$

$$c4s4 = c3 + a2b2; \quad (5)$$

The final result will be $c4s4s3s2s1s0$. This multiplication method is applicable for all the cases.

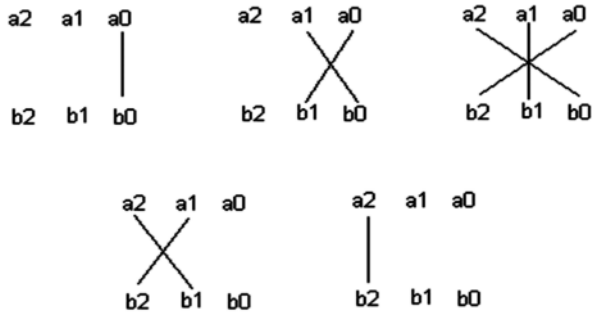

Figure 1: The Urdhva-tiryakbhyam Multiplication Method [2]

3. IMPLEMENTATION AND TESTING

The implementation of Vedic Multiplier is done using VHDL and the functionality of each block is verified using simulation software, ModelSim and ISE. The basic building blocks are two input AND gate and Adder, so the structural modeling style is used for the implementation of Vedic Multiplier.

A digital system is tested and diagnosed during its lifetime on numerous occasions. It is very critical to have quick and very high fault coverage testing. The self-test is commonly is used for testing of chips [4, 5, 6]. The basic idea of BIST, in its most simple form, is to design a circuit so that the circuit can test itself and determine whether it is "good" or "bad" (fault-free or faulty, respectively). This typically requires additional circuitry whose functionality must be capable of generating test patterns as well as providing a mechanism to determine if the output responses of the circuit under test (CUT) to the test patterns correspond to that of a fault-free circuit. The basic architecture of BIST is shown in the Figure 2.

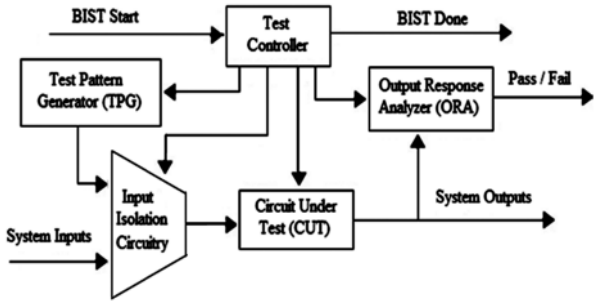

Figure 2: Basic BIST Architecture

The two essential functions include the test pattern generator (TPG) and output response analyzer (ORA). While the TPG produces a sequence of patterns for testing the CUT, the ORA compacts the output responses of the CUT into some type of Pass/Fail indication. The other two functions needed for system-level use of the BIST include the test controller (or BIST controller) and the input isolation circuitry. Aside from the normal system I/O pins, the incorporation of BIST may also require additional I/O pins for activating the any BIST sequence (the BIST Start control signal), reporting the results of the BIST (the Pass/Fail indication), and an optional indication (BIST Done) that the BIST sequence is complete and that the BIST results are valid and can be read to determine the fault-free/faulty status of the CUT [5,6,7].

4. RESULT AND CONCLUSION

In this paper we are evaluating the performance of the proposed high speed low power Vedic multiplier by comparing this design with a conventional Array Multiplier and Booth Multiplier. These multipliers are implemented using VHDL In order to get the power report and delay report the multipliers are synthesized using Xilinx ISE tool and Spartan 2E FPGA is used. Table 1 compares the simulation result of multipliers with Vedic Multiplier on basis of time delay and power.

Table 1
Comparison Between Multipliers

Multiplier Type	*Multiplier*	*FPGA Type*	*Delay ns Power Dissipation mW*
Array Multiplier [8]	Spartan 2	14.886	40
Booth Multiplier	Spartan 2	15.092	35
Vedic Multiplier	Spartan 2	6.801	31

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