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Comparative Analysis and Characterization of a Current Conveyor-II

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ABSTRACT

This paper introduces two different CCII circuits: one is based on current mirrors [1], and second is based on a differential pair [1]. The authors have simulated above two configurations using AMS 0.5 µm CMOS technology and the results are also tabulated for comparison. The authors have measured terminal impedances, gain, bandwidth and offset using Eldo SPICE tool.

Keywords: CCII, Current Mirror, Differential Pair

1. INTRODUCTION

In voltage mode circuits, the main building block used to add subtract, amplify, attenuate, and filter voltage signals is the operational amplifier. In current-mode circuits, the analogous building block is the current conveyor. Current conveyors and related current-mode circuits have begun to emerge as an important class of circuits with properties that enable them to rival their voltage-mode counterparts in a wide range of applications. The use of current rather than voltage as the active parameter can result in higher usable gain, accuracy and band-width due to reduced voltage excursion at sensitive nodes. Current conveyors are unity gain active elements exhibiting high linearity, wide dynamic range and high frequency performance than their voltage mode counterparts. A current-mode approach is not just restricted to current processing, but also offers certain important advantages when interfaced to voltage-mode circuits.

2. CURRENT CONVEYOR

From their introduction in 1968 by Smith and Sedra [4] and subsequent reformulation in 1970 by Sedra and Smith [5], current conveyors have proved to be functionally flexible and versatile, rapidly gaining acceptance as both a theoretical and practical building block. CCII is a three terminal device, schematically represented as under [1]:

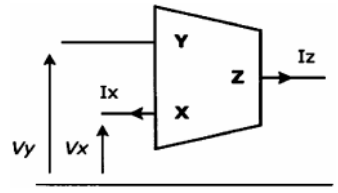

Fig 1: CCII Block Representation

The electrical characteristics of CCII can be shown using matrix as under [1]:

$$\begin{bmatrix} I_Y \\ V_X \\ I_Z \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 \\ 1 & 0 & 0 \\ 0 & \pm 1 & 0 \end{bmatrix} \begin{bmatrix} V_Y \\ I_X \\ V_Z \end{bmatrix}$$

CCII Node	*Impendance level*
X	Low (ideally 0)
Y	High (ideally ∞)
z	High (ideally ∞)

Fig 2: CCII Main Characteristics

The output current I_Z thus depends only on the input current at terminal X, in Fig. 1. This current may be injected directly at X, or it may be produced by the copy of the input voltage V_Y, from terminal Y, acting across the impedance connected at X. In a class II current conveyor input Y draws no current, whereas, for the older class I formulation, the impedance connected at X is also reflected at Y. The + sign indicates whether the conveyor is formulated as an inverting or non-inverting circuit, termed CCII- or CCII+. By convention, positive is taken to mean I_X and I_Z both flowing simultaneously towards or away from the conveyor [6].

3. CHARACTERIZATION OF CCII

3.1. Class AB CCII based on Current Mirrors

In this circuit, IBias1 and IBias2 have to be equal [7, 8]. Considering the products $g_m r_0$ much greater than 1, the voltage characteristic is very close to the ideal one [1]. In fact:

$$\alpha = \frac{V_X}{V_Y} = \frac{1}{1 + \frac{1}{(g_{m_2} + g_{m_4})(r_{o2} // r_{o4})}} \cong 1 \quad (1)$$

Considering loads connected to X and Z nodes to be negligible and $g_m r_o >> 1$, β can be given as:

$$\beta = \frac{I_Z}{I_X} \cong \frac{g_{m_2} g_{m_6} g_{m_7} + g_{m_4} g_{m_5} g_{m_8}}{g_{m_5} g_{m_6} (g_{m_2} + g_{m_4})} = 1 \quad (2)$$

if $g_{m_5} = g_{m_7}$ and $g_{m_6} = g_{m_8}$.

The impedance level at *Y* node can be ensured by employing good biasing sources showing high resistances as:

$$Z_Y = \left(\frac{r_{01}}{1 + g_{m_1} r_{01}} + R_{1B1AS1}\right) // \left(\frac{r_{02}}{1 + g_{m_2} r_{02}} + R_{1B1AS2}\right)$$
$$\cong \frac{R_{1B1AS1}}{R_{1B1AS2}} \quad (3)$$

The *X* node impedance can be obtained by neglecting some components as:

$$Z_X \cong \frac{1}{g_{m_2} + g_{m_4} + \frac{r_{02} + r_{04}}{r_{02} r_{04}}} \cong \frac{1}{g_{m_2} + g_{m_4}}$$

The impedance seen at *Z* node is typically high and it is given by:

$$Z_Z = \frac{r_{07} r_{08}}{r_{07} + r_{08}} \quad (5)$$

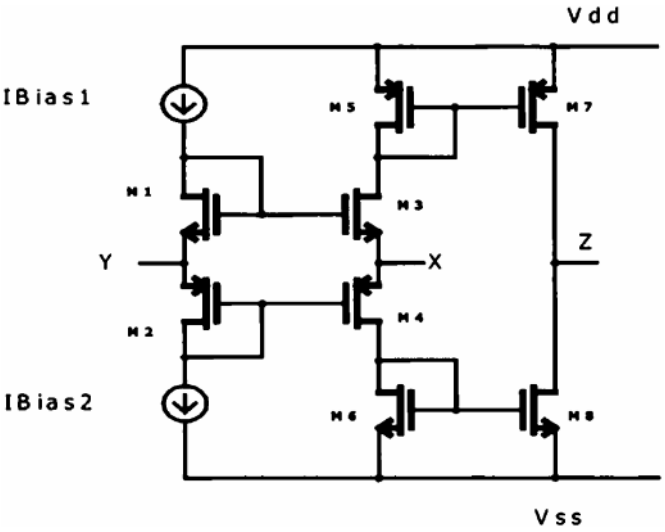

Fig 3: CCII based on Current Mirrors

3.2. Class AB CCII based on a Differential Pair

In this circuit, if the MOS output resistance is negligible, the voltage transfer error á is always close to unity [1].

$$\alpha = \frac{V_X}{V_Y} = \frac{\frac{r_{05} r_{06}}{r_{05} + r_{06}} (g_{m5} + g_{m6}) \frac{r_0}{2} g_{m2}}{\frac{r_{05} r_{06}}{r_{05} + r_{06}} (g_{m5} + g_{m6}) \frac{r_0}{2} g_{m1} + 1}$$
$$\cong \frac{g_{m2}}{g_{m1}} \quad (6)$$

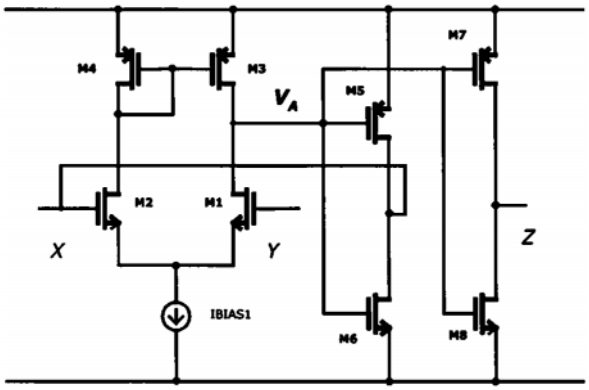

Fig 4: CCII based on a Differential Pair

If the load resistances are not very high compared to the MOS output resistances, the current transfer β is given as [1]:

$$\beta = \frac{I_Z}{I_X} \cong \frac{g_{m2} + g_{m7}}{g_{m6} + g_{m5}} \quad (7)$$

The parasitic impedance at *Y* node is given only by the input transistor gate. Its value is easily evaluated knowing transistor sizes and the unitary capacitance of the input gate [1].

$$Z_Y = \gamma W(M1) L(M1) C_{OX} \quad (8)$$

The *X* node impedance is inductive. Its resistance part is given by [1]:

$$R_X = \frac{1}{\frac{r_{05} + r_{06}}{r_{05} r_{06}} + g_{m2} \frac{r_0}{2} (g_{m5} + g_{m6})}$$
$$\cong \frac{2}{g_{m2} r_0 (g_{m5} + g_{m6})} \quad (9)$$

and its inductive part is given by:

$$L_X \cong \frac{\frac{z}{p_0}}{g_{m2} r_0 (g_{m5} + g_{m6})} \quad (10)$$

The *Z* node impedance is high because it is a parallel of two transistor output resistances [1].

$$Z_Z = \frac{r_{07} r_{08}}{r_{07} + r_{08}} \quad (11)$$

4. PRE-LAYOUT SIMULATION RESULTS

Pre-layout simulations are carried out in Eldo Spice tool of Mentor Graphics for all circuits. Different

characteristics such as gain, bandwidth, terminal impedances and offsets are observed in AMI 0.5µm technology.

4.1. Class AB CCII based on Current Mirrors

Power consumption = 208 µW

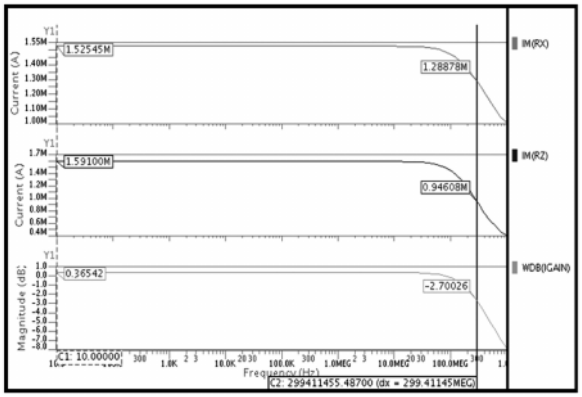

Fig 5: Gain and Bandwidth

We obtain the current gain of 0.36dB and the Bandwidth of 299 MHz as shown in fig.5. To obtain unity voltage gain between Y and X terminals, the output impedances of M3 and M4 should be very high.

As per the basic requirement of CCII characteristics, the impedance at X terminal is low (1.58KΩ) and it becomes inductive at higher frequency as shown in fig.6.

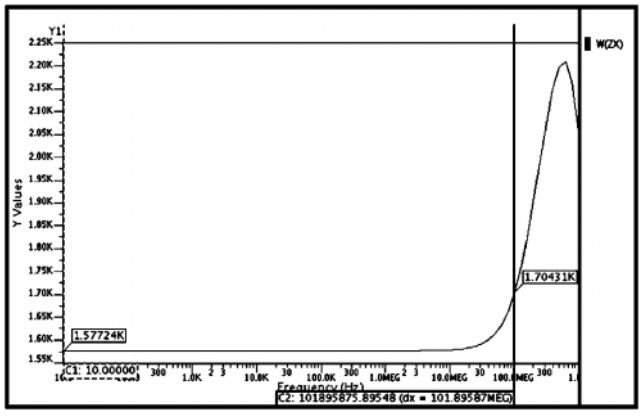

Fig 6: *X* Node Impedance

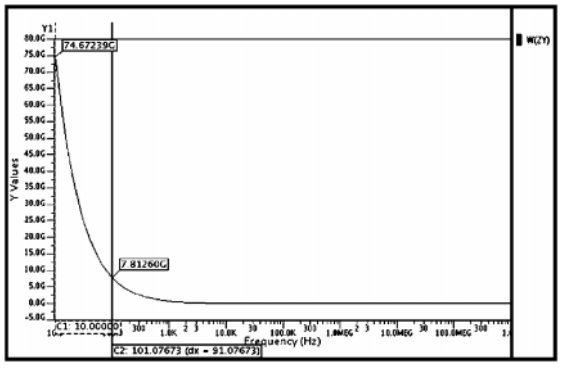

Fig 7: *Y* Node Impedance

The *Y* node impedance is very high (74.67GΩ) and it is capacitive as shown in Fig.7. It depends on resistances of current sources.

The Z node impedance is very high (129KΩ) and it is capacitive at higher frequency as shown in Fig.8.

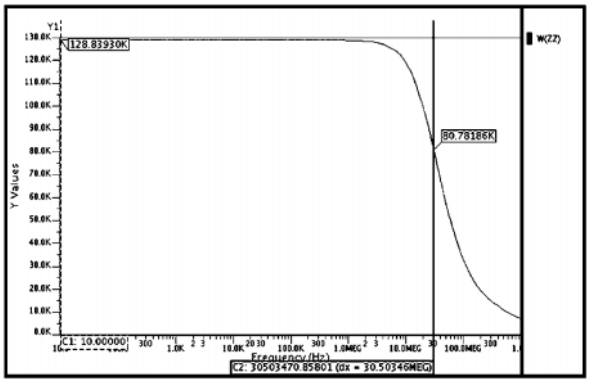

Fig 8: Z Node Impedance

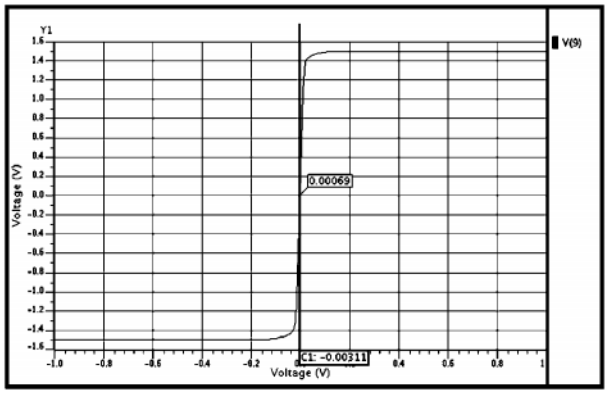

Fig 9: Offset Measurement

4.2. Class AB CCII based on a Differential Pair

Power consumption = 3.83 mW

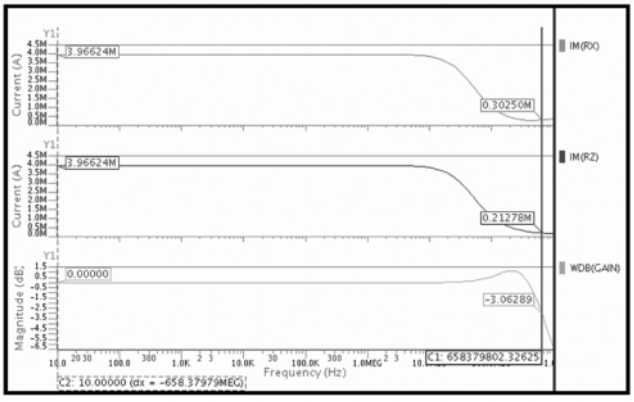

Fig 10: Gain and Bandwidth

Here we obtain the unity gain with 658MHz bandwidth which is very high compared to CCII based on current mirrors. The biasing current required is also low (10µA) compared to CCII based on current mirrors.

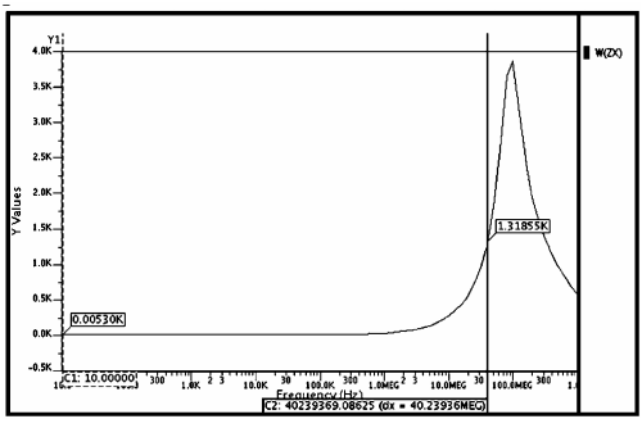

Fig 11: *X* Node Impedance

The X node impedance is low (5.30Ω) because of feedback through M5 transistor. It is inductive at high frequency.

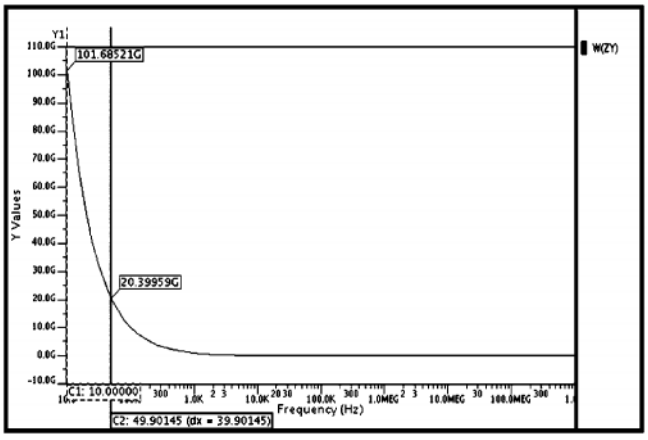

Fig 12: *Y* Node Impedance

The Y node impedance is very high (101.68GΩ) which depends on input transistor size. It is capacitive as shown in Fig.12.

The *Z* node impedance is also high (17.89KΩ) which depends on output resistances of M7 and M8.

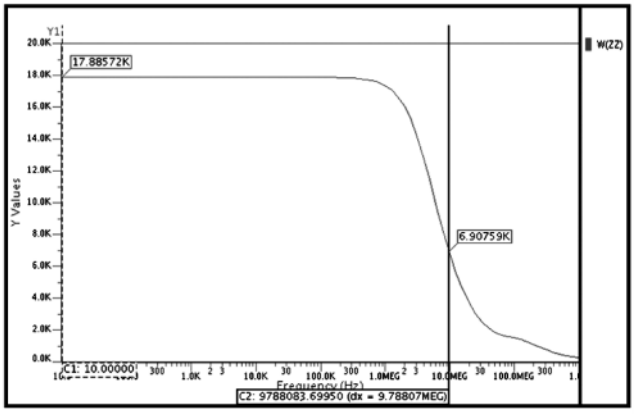

Fig 13: Z Node Impedance

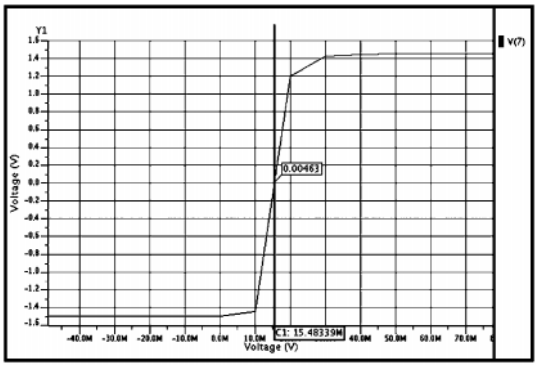

Fig 14: Offset Measurement

Table
1 Simulated Results of Both above Circuits in 0.5µm Technology

Current Conveyor Characteristics		
Data & Parameters	*Simulated Values in 0.5µm*	
	CCII based on CM	CCII based on Diff. Pair
Voltage Supply	±1.5V	±1.5V
Power Consumption	208µW	3.83mW
3dB Bandwidth	299MHz	658MHz
Biasing Current IBIAS	26µA	10µA
Offset	-3.1mV	15.48mV
Current Gain(â)	0.36dB	0dB
Node Y Parasitic Impedance	74.67GΩ	101.68GΩ
Node X Parasitic Resistance	1.58KΩ	5.30Ω
Node X Parasitic Inductance	2.66µH	5.22µH
Node Z Parasitic Resistance	129KΩ	17.89KΩ
Node Z Parasitic Capacitance	0.065pF	2.35pF

5. POST LAYOUT SIMULATION

Layouts and Post layout simulations of CMOS Current Conveyors are carried out in AMI 0.5µm technology using Eldo spice and IC station in Mentor Graphics.

5.1. Class AB CCII based on Current Mirrors

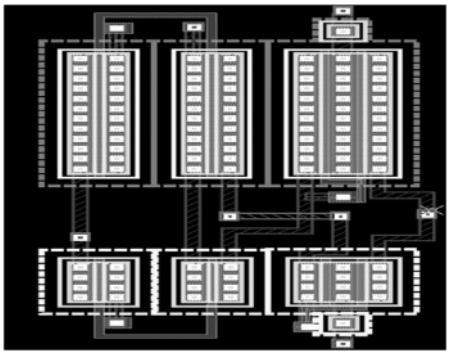

Fig 15: Layout of CCII based on Current Mirrors in 0.5µ Technology

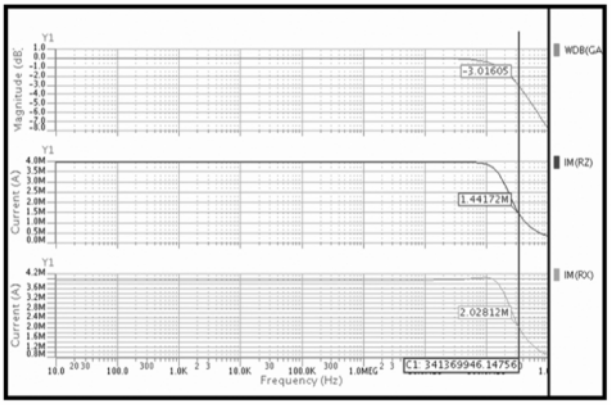

Fig 16: Gain and Bandwidth

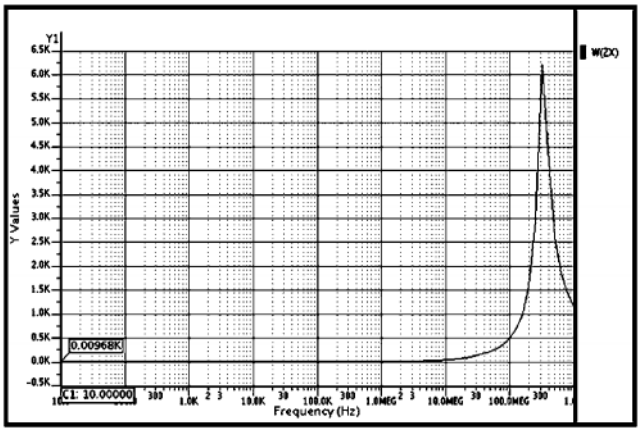

Fig 17: X Node Impedance

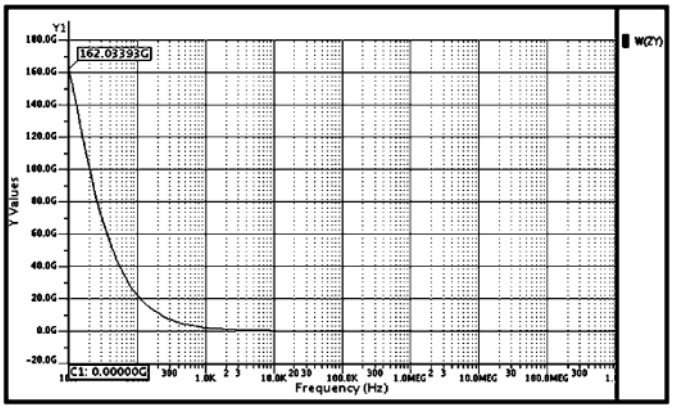

Fig 18: Y Node Impedance

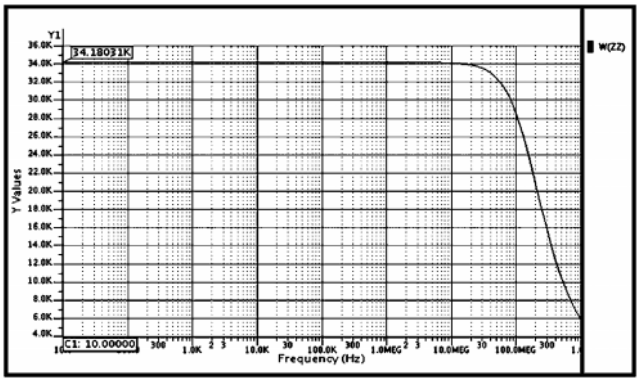

Fig 19: Z Node Impedance

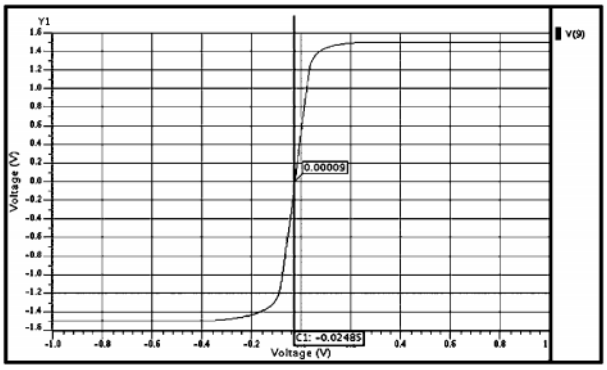

Fig 20: Offset Measurement

5.2. Class AB CCII based on a Differential Pair

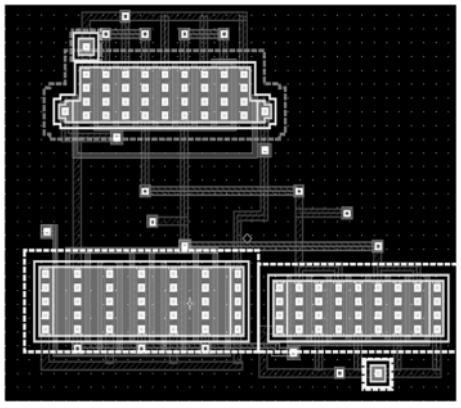

Fig 21: Layout of CCII based on Differential Pair in 0.5µ Technology

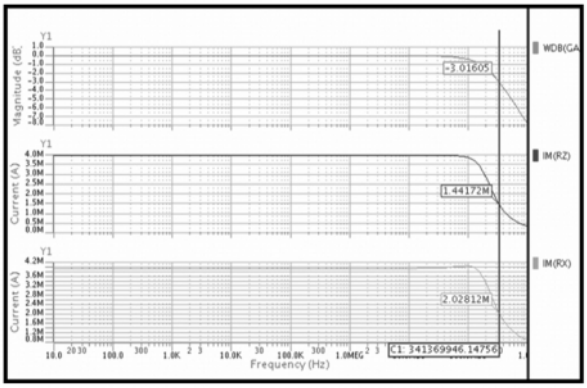

Fig 22: Gain and Bandwidth

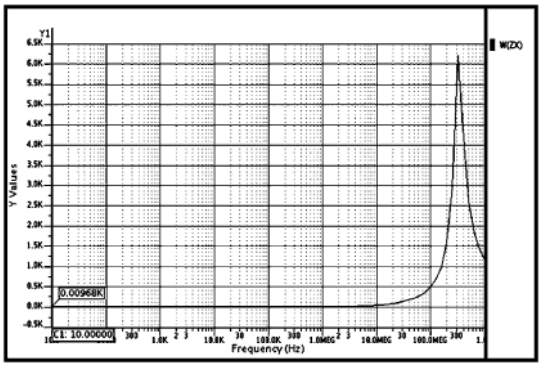

Fig 23: X Node Impedance

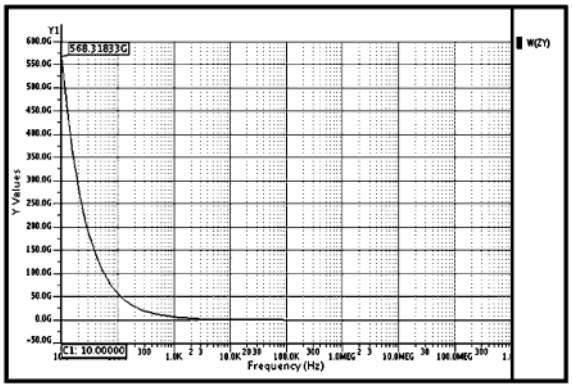

Fig 24: Y Node Impedance

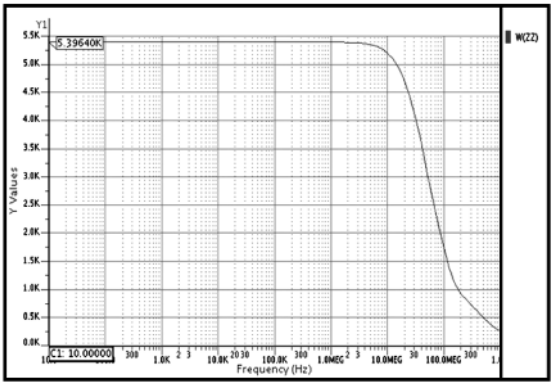

Fig 25: Z Node Impedance

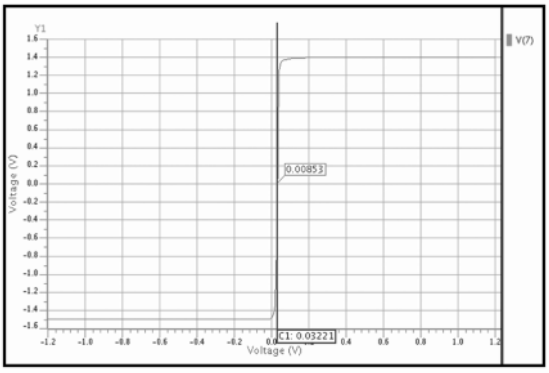

Fig 26: Offset Measurement

6. CONCLUSION

Both CMOS current conveyors are designed with AMI 0.5µm technology. Layouts are designed in IC station in Mentor Graphics. Pre-layout and Post-layout simulations are performed in Eldo spice tool. The second generation current conveyor based on differential pair gives better bandwidth and terminal impedances with reduced biasing current requirement compared to second generation current conveyor based on current mirrors.

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